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Heiman and Hofstein[4] have described another insulated-gate field-effect transistor which is formed in the surface of a single crystal of silicon. Although some of the physical mechanisms of the two insulated-gate devices are similar, differences in the nature of the semiconductor and the structure produce differences in the operating characteristics. Thin-film transistors using evaporated cadmium selenide as the semiconductor have been reported by Shallcross[5] of these Laboratories.

The construction of an insulated-gate thin-film transistor is shown in Figure 1. The gold source and drain electrodes are deposited by

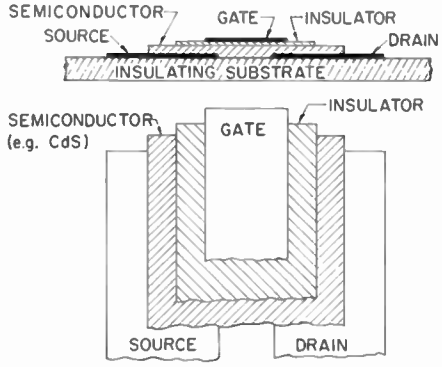

Fig. 1—Cross section and cut-away plan view of a TFT. The thickness of the layers is exaggerated compared to the lateral dimensions.

evaporation through a mask onto an insulating substrate, such as glass. Typical experimental units have electrodes 100 mils long separated by a gap of about 0.4 mil (10 microns). The semiconductor consists of an evaporated layer of polycrystalline n-type cadmium sulfide less than 1 micron thick. On top of the CdS layer, a thin film of insulator usually less than 0.1 micron thick is deposited by evaporation. Typical insulator materials found to be suitable are silicon monoxide or calcium fluoride. The gate electrode, a thin film of aluminum or gold approximately 15 microns wide, is evaporated on top of the insulator and centered over the source–drain gap. In the structure shown the gate slightly overlaps the source and drain electrodes. The thicknesses of the various layers have been exaggerated in the figure; the actual gap width is about 20 times the thickness of the CdS layer.

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[4] F. P. Heiman and S. R. Hofstein, "The Insulated-Gate Field-Effect Transistor," presented at Electron Devices Meeting, Washington, D. C., Oct. 1962 (to be published).

[5] F. V. Shallcross, "Cadmium Selenide Thin-Film Transistors," *Proc. I.E.E.E.*, Vol. 51, p. 851, May 1963.

Due to the presence of the insulator layer, the gate may be biased either positively or negatively with respect to the source without drawing appreciable gate current. Typical d-c input resistance is 10 megohms or more. TFT's have been processed so that only a very small source–drain current flows at zero gate voltage. However, this small current is enhanced by several orders of magnitude when positive gate voltage is applied. The increase in current is due to the formation by field effect of a conducting channel in the cadmium sulfide adjacent to the under-surface of the insulator.

Drain Characteristics

A typical drain characteristic of such an "enhancement" unit is shown in Figure 2. The drain current is plotted as a function of drain

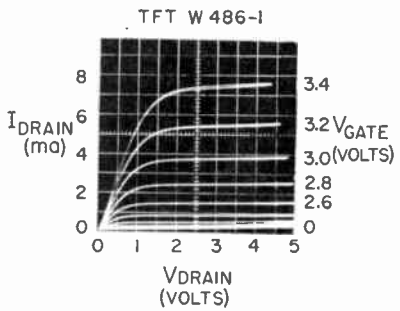
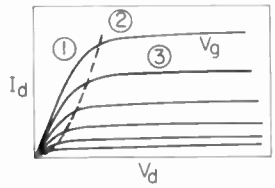


Fig. 2—The drain characteristic of an experimental enhancement-type cadmium sulfide TFT. The maximum transconductance of this unit is about 10,000 μmhos.

voltage with the gate voltage as a parameter. All voltages indicated are positive with respect to the source. Note that the device exhibits pentode-like characteristics. Since a 0.2-volt change on the gate produces a 2-milliampere change in drain current, the transconductance of this unit is about 10,000 micromhos. The dynamic output resistance determined by the reciprocal of the slope of the curves in the saturation region is about 8,000 ohms. The voltage amplification factor calculated from the product of the transconductance and output resistance is 80.

The saturated characteristics result from the pinch-off of the induced conduction channel in the region of the drain. The rising potential along the channel from source-to-drain relative to the gate potential causes a gradation from an accumulation layer near the source to a depletion layer near the drain. The saturation mechanism is thus a gate-control phenomenon quite analogous to that observed in the conventional field-effect transistor.

Insulated-gate TFT's have also been produced which operate in the "depletion" mode. Such units exhibit saturated characteristics with sizeable drain current flowing when the gate is at the same potential as the source. This drain current may be depleted by applying negative gate voltage or enhanced by positive gate voltage. The drain characteristic is similar to the one shown in Figure 2 except for the gate voltage scale.



① $G_d \propto V_g + K_1$

② $V_{d\,KNEE} \propto V_g + K_2$

③ $I_d \propto (V_g + k_3)^2 \quad \therefore \quad g_m \propto \sqrt{I_d}$

Fig. 3—Typical TFT drain characteristics. The dashed line (2) represents the locus of the knees of the curves.

Enhancement units, such as the one shown, are of interest for integrated-circuit applications[2,6] because the positive gate bias permits direct coupling of successive stages. The depletion units are useful for input, detector, and other applications where zero bias is desirable.

Figure 3 shows the behavior of drain characteristics of both enhancement- and depletion-type TFT's. The drain characteristic illustrated has been separated into two regions by the dashed line. In region (1) at low drain voltage, below the onset of current saturation, the output conductivity is found to be linear with the gate voltage. The dashed line (2) represents the locus of the knees of the curves. It has been found that at the knee, there is a linear relationship between the drain voltage and the gate voltage. Region (3) is the high-drain-voltage, current-saturation area. Here there is a square-law dependence of the drain current on the gate voltage. A consequence of this last characteristic is that the transconductance is proportional to the square root of the drain current. All three of the characteristics mentioned above are typical of these types of experimental TFT's.

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[6] P. K. Weimer, "Evaporated Circuits Incorporating Thin-Film Transistors," presented at International Solid-State Circuits Conference, Philadelphia, Pennsylvania, Feb. 1962.

Comparison of Calculated and Measured Characteristics

An analysis of the TFT structure based solely on the field-effect phenomenon is given in the appendix. The analysis assumes that the semiconductor is a thin homogeneous layer with constant mobility, and that the source and drain electrodes form ohmic contacts to the semiconductor. The expression for the drain characteristic below the onset of current saturation is, as shown in the Appendix,

$$I_d = \frac{\mu C_g}{L^2}\left[(V_g - V_0)\, V_d \frac{V_d^2}{2} \right], \tag{1}$$

where I_d = drain current in amperes,

μ = drift mobility in cm²/volt-sec,

C_g = capacitance across insulator layer ≈ total gate capacitance, in farads,

L = length of gap between source and drain electrodes,

V_0 = gate voltage required for the onset of drain current,

V_g = applied gate voltage relative to the source electrode,

V_d = applied drain voltage relative to the source electrode.

Note that V_0 is positive for an enhancement-type unit, which requires an initial gate bias to fill immobile surface states and/or traps in the forbidden band of the semiconductor. V_0 is negative in a depletion-type unit having an initial conductivity at zero gate bias. Equation (1) is valid for $V_d \leq V_g - V_0$, up to the knee in the I_d versus V_d characteristic. Shockley[3] has shown that the drain current is constant, independent of the drain voltage above the knee of the curves in the drain characteristic. The theoretically predicted drain characteristic obtained from Equation (1) appears in Figure 4.

Three experimentally determined traits of drain characteristics, shown in Figure 3, may now be compared with the theoretically predicted traits. The output conductivity below the knee is

$$G_d = \left.\frac{\partial I_d}{\partial V_d}\right|_{V_d \to 0} = \frac{\mu C_g}{L^2}(V_g - V_0), \tag{2}$$

i.e., the output conductivity is linear with V_g.

The locus of the knees of the curves is determined from the zero-slope condition of Equation (1). It is found that the drain voltage at the knee is

$$V_{d(\text{knee})} = V_g - V_0. \tag{3}$$

The drain voltage at the knee is *equal* to the effective gate voltage. Since experimental TFT's may have a shunting source–drain resistance which tilts the drain characteristics upward slightly, it is difficult to

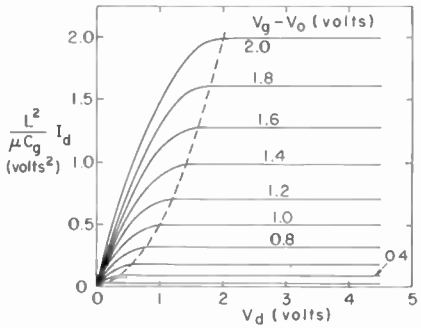

Fig. 4—Theoretically predicted TFT drain characteristics. These curves result from an analysis based solely on field-effect. The dashed line is the locus of the knees of the curves.

uniquely determine the drain voltage at the knee and verify Equation (3). However, the uncertainty of the locus of points down from the knee by a constant factor, $y < 1$, is small and was used to determine the experimental relationship; the voltage at the knee is *proportional* to the quantity gate voltage plus a constant. The corresponding expression for the modified voltage at the knee is

$$V_{d'(\text{knee})} = (1 - \sqrt{1-y})\,(V_g - V_0), \tag{4}$$

which verifies the *proportionality* relationship.

The maximum drain current (at the knee), determined from Equations (1) and (3) is,

$$I_{d(\max)} = \frac{\mu C_g}{2L^2}\,(V_g - V_0)^2, \tag{5}$$

which verifies the experimentally found square-law relationship of

saturated drain current with the effective gate voltage. The transconductance of this device at or above the knee is given by,

$$g_m = \left.\frac{\partial I_{d(\max)}}{\partial V_g}\right|_{V_d=\text{const.}} = \frac{\mu C_g (V_g - V_0)}{L^2} = \frac{\sqrt{2\mu C_g I_{d(\max)}}}{L}, \quad (6)$$

or, the transconductance is proportional to the square root of the drain current.

Therefore, all three of the experimentally determined traits of drain characteristics of experimental enhancement and depletion type TFT's have been predicted by a field-effect analysis of a simple model. This provides good evidence that the primary operating mechanism in the TFT is conductivity modulation of the channel by field effect.

A figure of merit which characterizes the high-frequency performance of a three-terminal active device is its gain–bandwidth product. For the TFT it can be shown that

$$\text{gain} \times \text{bandwidth} \approx \frac{g_m}{2\pi C_g}. \quad (7)$$

Typical experimental units have demonstrated gain–bandwidth products of about 15 megacycles. The calculated figure of merit determined from Equation (1) (which applies at or below the knee) yields,

$$\text{gain} \times \text{bandwidth} \approx \frac{\mu V_d}{2\pi L^2}, \quad (8a)$$

while Equation (6) (which applies at or above the knee) yields,

$$\text{gain} \times \text{bandwidth} \approx \frac{\mu (V_g - V_0)}{2\pi L^2}. \quad (8b)$$

Of course, these two expressions are identical at the knee through Equation (3). One may determine the effective drift mobility in the semiconductor from either Equation (8a) or (8b) by inserting the measured gain–bandwidth product, length of source–drain gap and appropriate voltage. This yields an effective drift mobility of about 100 cm^2/volt-sec for this 15-megacycle unit.

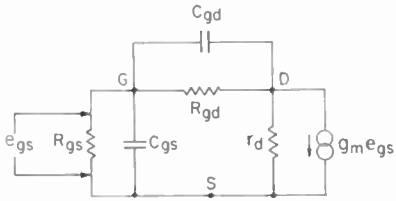

Fig. 5—TFT small-signal equivalent circuit.

Impedance Considerations

The small-signal equivalent circuit of a TFT may be represented as shown in Figure 5. The gate, drain, and source electrodes are represented as the nodal points marked G, D, and S. The impedances between gate-and-source and gate-and-drain electrodes are represented by parallel *RC* circuits. As will be shown, the magnitude of these impedances are dependent upon the d-c operating point and also upon the frequency. The output circuit consists of the dynamic output resistance, r_d, driven by a constant current generator, $g_m e_{gs}$. Drain–source capacitance is small and has been neglected.

The impedances between the elements in a TFT have been measured by several different techniques and the results found to be consistent. Figure 6 shows the total gate capacitance, C_g, measured between the gate and both the source and drain electrodes. C_g is plotted as a function of gate-to-source voltage with drain-to-source voltage as a parameter. As is shown in the transfer characteristic in the lower part of the figure, the unit illustrated is of the depletion type. Approximately 1 milliampere drain current flows at zero bias condition. Note that with zero drain volts applied, the capacitance increases and tends to level off as the gate potential increases in the positive direc-

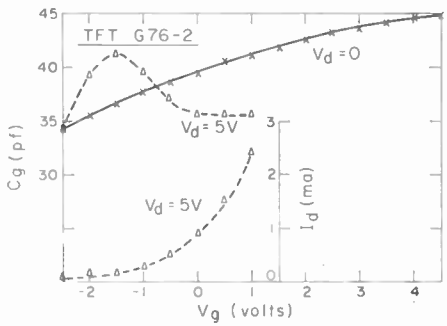

Fig. 6—Total gate capacitance and transfer characteristics of an experimental depletion-type cadmium sulfide TFT. The capacitance was measured at 100 kilocycles.

tion. However, at higher drain voltages it is found that the capacitance increases, reaches a maximum, and then decreases with gate voltage. This behavior has been observed repeatedly in both enhancement and depletion TFT's; the peak in capacitance being shifted toward positive gate biases for the enhancement units. The maximum in capacitance always seems to occur at a gate voltage which produces a drain current of about 5-10% of its maximum stable value. The data presented were taken at 100 kilocycles using a capacitance bridge. Other measurements taken at frequencies between 2 and 200 kilocycles have shown similar results except that the measured capacitance decreases slightly at the higher frequencies. Since the fall-off of capacitance at high

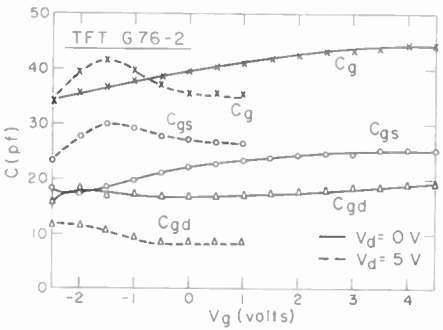

Fig. 7—Distribution of gate capacitance between source and drain electrodes of a cadmium sulfide TFT. All data points were measured independently.

drain voltage is observed over a wide range of frequencies and since the shunt resistance is large (as discussed shortly), the effect is due to a change in capacitance within the TFT. However, from the applications point of view, it does not matter whether the cause is due to a capacitance or a resistance change, since the input signal will see the capacitance and shunt resistance as measured in these tests.

Three-terminal capacitance measurements are used to determine the isolated capacitances and shunt resistances which exist between two of the three terminals of the TFT. The results of such measurements are shown in Figure 7. The solid-line curves correspond to zero drain voltage, while the dashed curves are for 5 volts applied to the drain. The total gate capacitance, C_g, is separated into two components: C_{gs}, the capacitance between gate and source and C_{gd}, the capacitance between gate and drain. Note that with both source and drain electrodes grounded, the total gate capacitance divides about equally between the gate–source and gate–drain regions. However, at higher drain voltage (in the saturation region) the major portion of gate

capacitance, including the peaked characteristic, exists in the gate-source circuit and only a relatively small amount in the gate-drain circuit. This situation is desirable because in TFT amplifier applications, it is the gate–drain capacitance which is magnified by feedback. The distribution of shunt resistance from the gate to the source and drain electrodes also varies with operating voltages. At zero drain voltage the gate–drain and gate–source resistances are about equal and do not vary greatly with gate voltage. However, the gate–drain resistance increases and the gate–source resistance decreases as the drain voltage is increased. It has been found that these shunt resistances, measured at 100 kilocycles, are greater than about one megohm for the TFT being described.

The behavior of the gate capacitance as a function of gate voltage with zero volts applied to the drain is the result of the changing width of the space-charge region in the semiconductor adjacent to the insulator. The positive gate voltage narrows this width and at very high voltage the measured gate capacitance approaches the geometrical capacitance across the insulator. Of course, with both source and drain electrodes at the same potential, the total gate capacitance should be distributed between these two electrodes geometrically. In this sample the measured total gate capacitance increased by about 35% over the voltage range. This is a typical value, with the maximum observed increase being about 100%. These numbers suggest that the maximum width of the space-charge region is about comparable to the width of the insulator layer. However, in the operating range it is much less than the insulator thickness. In effect, a conductive channel is built into the upper surface of the semiconductor. The analysis given in the Appendix still applies with the modification that the effective semiconductor thickness, h, becomes the thickness of the space-charge region and not the total semiconductor thickness.

At high drain voltage in the current-saturation region, the observed fall-off in capacitance with the onset of drain current may be explained by the repulsion of the induced channel away from the gate in the neighborhood of the drain. Since the potential of the channel must rise from source to drain, a gradation from an accumulation layer in the vicinity of the source to a depletion layer near the drain is developed. However, impedance-wise the channel is connected more closely to the source than to the drain, causing the bulk of the gate capacitance to appear between gate and source electrodes rather than between gate and drain.

ACKNOWLEDGMENTS

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V. L. Frantz, R. R. Goodrich, W. S. Homa, H. P. Lambert, L. Meray-Horvath, and R. G. Pugliesi for construction and testing of the experimental TFT's and associated equipment. The discussions with H. Johnson, D. O. North, A. Rose, and F. V. Shallcross have been most valuable. In particular, the authors are indebted to A. Many for his contribution to the field-effect analysis.

Appendix — Field-Effect Analysis of the TFT Structure

The following analysis of the thin-film transistor, which predicts the drain characteristic expected solely from the effect of electric fields

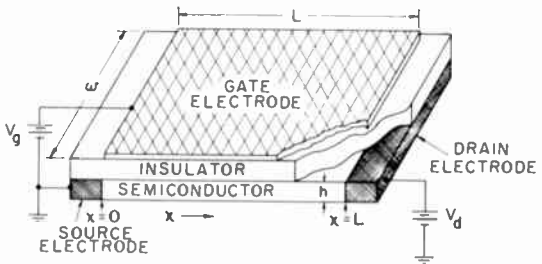

Fig. 8—TFT structure used for analysis.

produced by the potentials applied to the electrodes, is based upon unpublished work of A. Many. It differs from an analysis by Ihantola[7] for the metal-oxide–semiconductor transistor in that the initial charge density is taken into account. In this analysis one assumes a homogeneous layer of semiconductor thin compared to the insulator, having constant mobility, and forming ohmic contacts with the source and drain electrodes. Only majority carriers are considered to exist in the semiconductor. A somewhat similar analysis applicable to the unipolar field-effect transistor was presented by W. Shockley.[3]

As is shown in Figure 8, the semiconductor is a film having a thickness, h; length of gap between source and drain electrode, L; and width, w. The gate electrode is spaced from the semiconductor by an insulating layer, and capacitance C_g exists across this insulator. In this analysis C_g is assumed constant even though measurements of total gate capacitance on TFT's indicate some variation with operating voltages. The potential of the semiconductor at an arbitrary point x,

[7] H. K. J. Ihantola, "Design Theory of a Surface Field-Effect Transistor," ASD Technical Note 61-133, Sept. 1961.

measured from the source electrode, is given by $V(x)$. The potentials applied to the gate and drain electrodes relative to the source electrode are V_g and V_d. With $\Delta N(x)$ charges per unit area impressed onto the gate electrode, an equal number of charges of q coulombs per charge is induced in the semiconductor. The charge induced per unit area is given by,

$$q\Delta N(x) = \frac{C_g}{wL}[V_g - V(x)]. \tag{9}$$

The drain current, I_d, in the semiconductor may be expressed as

$$I_d = hw\mu q\left[\frac{N_0}{hwL} + \frac{\Delta N(x)}{h}\right]E_x, \tag{10}$$

where μ = drift mobility in cm^2/volt-sec,

E_x = electric field in volts/cm,

N_0 = total number of initial charges in the semiconductor.

This drain current expression may be written as

$$I_d = \frac{\mu q}{L}\left\{N_0 + \frac{C_g[V_g - V(x)]}{q}\right\}\frac{dV(x)}{dx}, \tag{11}$$

$$I_d\int_0^L dx = \frac{\mu C_g}{L}\int_0^{V_d}\left[\frac{N_0 q}{C_g} + V_g - V(x)\right]dV(x), \tag{12}$$

which yields

$$I_d\mathrm{L} = \frac{\mu C_g}{L}\left[\left(\frac{N_0 q}{C_g} + V_g\right)V_d - \frac{V_d^2}{2}\right]. \tag{13}$$

The term N_0q/C_g may be replaced by a voltage $-V_0$, where $+V_0$ represents the gate voltage required for the onset of drain current. Note that V_0 is positive for an enhancement-type unit and negative for a depletion-type unit. Therefore, the drain current may be expressed as

$$I_d = \frac{\mu C_g}{L^2} \left[(V_g - V_0) V_d - \frac{V_d^2}{2} \right]. \qquad (1)$$

Equation (1) relates the drain current to both the drain and gate voltages. It is valid up to the point where the slope is zero, which corresponds to the knees of the characteristic curves.

MAGNETIC LOAD-SHARING SWITCHES FOR HIGH-SPEED APPLICATIONS

By

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Summary—The feasibility of driving a bidirectional diode matrix with load-sharing magnetic switches in high-speed applications is investigated. For purposes of analysis each switch core is treated as a pulse transformer. The necessary parameters of the pulse transformers are calculated by means of the source and load impedances and the pulse specifications. Experimental results are given for pulse transformers and a 3 × 3 diode matrix with magnetic storage elements as loads, driven by three magnetic load-sharing switches. The conclusions arrived at are: it is feasible to drive a bidirectional diode matrix with four load-sharing switches at 10 mc repetition rate; 5 mc operation is feasible with only two magnetic load-sharing switches.

Introduction

THE COST of a modern high-speed computer memory is greatly influenced by the cost of its electronic drive circuits. Transistors have limited current-delivering capability, and paralleling them to obtain greater currents and increased speeds is usually impractical. Furthermore, due to the memory organization, only a very small percentage of the drivers are excited and delivering current at any one time. Thus, a great deal of expensive equipment is idle most of the time. Matters are improved considerably if a number of drivers are used to deliver current simultaneously to a selected load. This is accomplished by means of magnetic load-sharing switches.

Magnetic matrix switches were described as early as 1952 by Rajchman.[1,2] The switch described in Reference (1) is based on a binary decoding scheme and is a load-sharing switch, since the output current of the selected matrix core is the sum of n input currents. A disadvantage of this early scheme is the excitation received by some of the unselected matrix cores. This excitation tends to drive these cores further into saturation, thereby producing spurious output signals and also increasing the driver load.

[1] J. A. Rajchman, "Static Magnetic Matrix Memory and Switching Circuits," *RCA Review*, Vol. 13, p. 183, June 1952.

[2] J. A. Rajchman, "A Myriabit Magnetic Core Matrix Memory," *Proc. I.R.E.*, Vol. 41, p. 1047, Oct. 1953.

Constantine[3] describes a load-sharing matrix switch with noise cancellation. The cancellation is obtained by the polarity pattern of the primary windings on the cores in combination with the drive pulses. This load-sharing switch is no longer a binary decoder; indeed, the number of input wires is larger than the number of output wires. The noise output of unselected cores depends on the tolerances in the amplitude and phase of the drive pulses, and is ideally zero.

The number of required input wires may in some cases be reduced as shown by Marcus.[4] A class of optimal noiseless load-sharing matrix switches which require a minimum of input wires are described by Chien.[5]

The present paper deals with the application of magnetic load-sharing switches in high-speed memories.

Operation of a Magnetic Load-Sharing Switch

A brief description of a load-sharing switch is given for the benefit of the reader unfamiliar with these devices. The diagram and the winding pattern of a four-input three-output switch are shown in Figure 1.

If an output pulse is to be generated, half of the input wires are excited. The core windings are arranged in such a fashion that the magnetic flux change due to the currents in the excited drive lines is zero in all unselected cores; thus these cores do not produce an output. All the drive currents flow in the same direction through the selected core. This core will be magnetized and current flows through the load that is connected to the output winding of the core. The magnetizing and load currents are distributed equally between the excited drive lines. Thus, the larger a switch is, the less current has to be delivered by a particular driver for a given output current amplitude. To select load "a" in Figure 1, lines 1 and 2 are excited. The applied current pulses may be positive or negative, depending on the desired output polarity. Thus, bi-directionality is achieved with one-polarity drivers only. If positive polarity drivers are used, a positive output pulse is generated at output "a" by exciting wires 1 and 2, and a negative output pulse by exciting wires 3 and 4.

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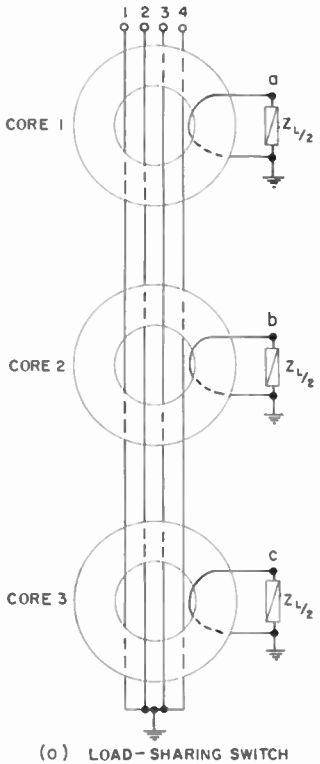
[3] G. Constantine, Jr., "A Load Sharing Matrix Switch," *I.B.M. Journal of Research*, p. 205, July 1958.

[4] M. P. Marcus, "Doubling the Efficiency of the Load Sharing Matrix Switch," *I.B.M. Journal of Research*, p. 195, April 1959.

[5] R. T. Chien, "A Class of Optimal Noiseless Load Sharing Matrix Switches," *I.B.M. Journal of Research*, p. 415, Oct. 1960.

Magnetic Load-Sharing Switch for High Speed

The purpose of this investigation is to establish the feasibility of a magnetic load-sharing switch for a 100-nanosecond (ns) cycle time memory. The width of the pulses to be delivered by the switch are assumed to be 30 ns. This means the pulse rise and fall times are to



CORE	INPUT WIRE			
	1	2	3	4
1	+	+	−	−
2	+	−	+	−
3	+	−	−	+

(b) WINDING PATTERN FOR (a)

Fig. 1—(a) Schematic diagram and (b) winding pattern of a four-input three-output switch.

be about 10 ns. It may be assumed that a drop of 10 per cent of the initial amplitude is tolerable.

For purposes of analysis, each matrix core may be treated as a pulse transformer. The effects of unselected cores on the drive lines are assumed negligible. Knowledge of the load impedance Z_L and source impedance, together with the pulse specifications, permits designing the required pulse transformers.

Load Impedance

It is assumed that magnetic load-sharing switches are used to drive a diode matrix with magnetic storage elements as loads (Figure 2a). A simplified equivalent circuit of the load to be driven by one pulse transformer is shown in Figure 2b. C_D represents the capacitance of the back-biased diodes which are connected to the selected drive line

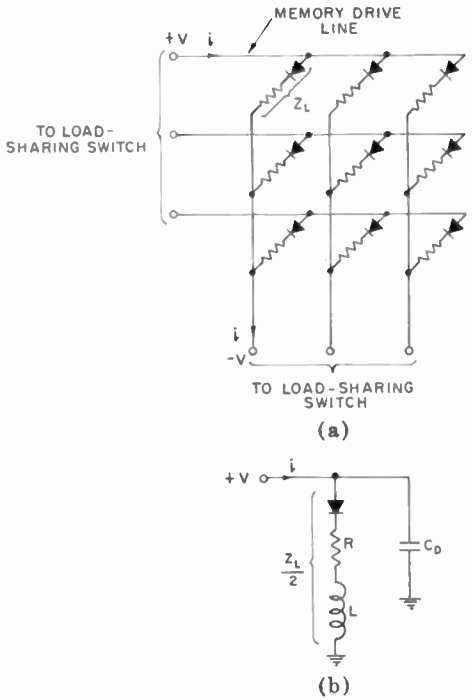


Fig. 2—(a) Diode matrix and (b) equivalent circuit of a selected drive line.

and the stray capacitance. R and L are that portion of the total load impedance, including the diode, which may be assumed to be driven from one load-sharing switch. This is symbolically indicated in Figure 1a. A more-detailed description of the diode matrix follows.

Equivalent Circuit for the Pulse Transformer

An approximate equivalent circuit for a pulse transformer is shown in Figure 3a, with all impedances referred to the primary. The distributed winding capacitances of the transformer are represented by a capacitor in parallel with the magnetizing inductance. The interwinding capacitance is neglected.

The performance of the transformer may be considered in three steps: (1) rise-time response, (2) flat-top response, and (3) fall-time response. For each one of these steps an even simpler equivalent circuit may be used as shown in Figures 3b and 3c for steps 1 and 2, respectively. The losses in the transformer core are also neglected in these equivalent circuits. It is next shown that core losses do not become excessive even at high repetition rates.

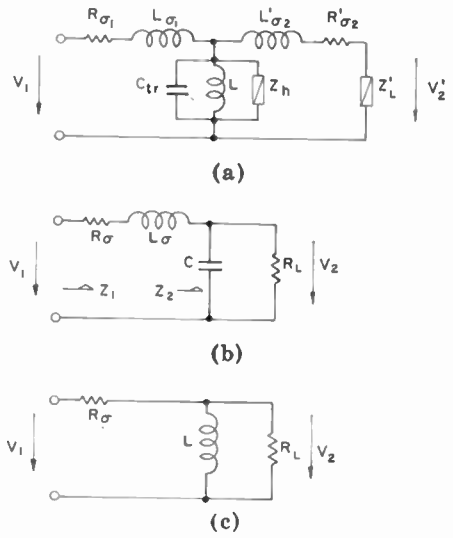


Fig. 3—(a) Equivalent circuit for a pulse transformer, (b) simplified equivalent circuit used for the calculation of the rise time response ($C = C_{tr} + C_D$), and (c) equivalent circuit used to calculate the flat-top response.

The core losses may be represented in the equivalent circuit by the elements shown in Figure 4b.[6] For ferrite cores with a very high resistivity, the eddy current losses may be neglected to a first-order approximation and only hysteresis losses need be considered. Linear ferrite material with a relative permeability of about 800 for 30-ns pulses is used, and the output voltage of the transformer is chosen to be 20 volts.

For the cores tested,* the following experimental results were ob-

[6] "Equivalent Circuit of a Pulse Transformer Core," Radiation Lab., MIT, Report 666, 1945.

* The ferrite material is composed of Fe_2O_3, NiO and ZnO. The core dimensions are: inner diameter = 2 mm, outer diameter = 8 mm, length = 6 mm.

tained (see Figure 4a):

$$\Delta B = .044 \text{ volt-second/square meter},$$
$$\Delta H = 9.1 \text{ amperes/meter},$$
$$2H_c = 3.9 \text{ amperes/meter}.$$

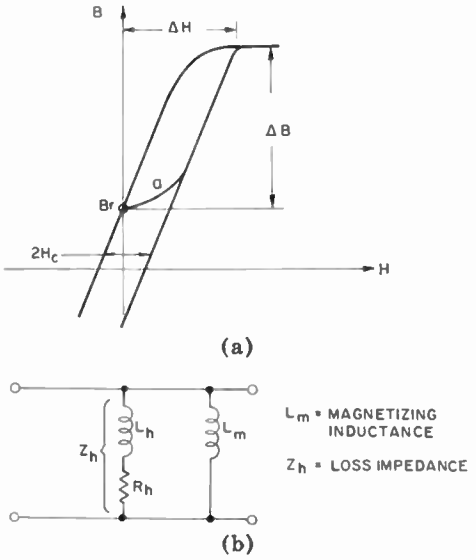


Fig. 4—(a) B-H loop of cores used and (b) equivalent circuit of a transformer core (eddy-current losses, etc., are neglected).

The cores require a current $I_{h\max}$ of 33 ma to produce a magnetic field of 3.9 amperes/meter. Hence

$$R_h = \frac{20}{33 \times 10^{-3}} \cong 600 \text{ ohms}.$$

R_h represents the real part of the hysteresis loss impedance. The rise time for the current which produced the field of $2H_c$ was found to be 15 nanoseconds. Thus, by means of the partial loop "a" in Figure 4a,

$$\tau \cong 10 \text{ ns}$$

and

$$L_h = \tau_h R_h = 6 \ \mu\text{h}.$$

The maximum hysteresis losses in a transformer core are found to be

$$P_h = 185 \text{ mw},$$

with a duty cycle of 30 per cent. Tests with pulses at 10 mc repetition rate showed that this power dissipation in the core does not heat up the core excessively.

A 1:1 primary-to-secondary turns ratio was chosen for the transformers. All the specifications needed to calculate the elements forming the lumped transformer equivalent circuit are now known. The load impedance given in Figure 2b may be represented by 20 ohms with 100 picofarads in parallel. The load capacitance is at least one order of magnitude larger than any capacitance intrinsic to the transformer, and this can be considered as some justification for the representation of all the capacitances by just one capacitor in parallel with the magnetizing inductance, especially if the stray impedances are combined as in Figure 3b. In that case, the load capacitance is in parallel with the transformer capacitance and the two may be combined.

Rise-Time Response

Referring to Figure 3b, the rise time response is calculated by use of the Laplace transformation;

$$Z_2 = \frac{R_L}{sR_LC + 1},$$

$$Z_1 = \frac{s^2R_LL_\sigma C + s\,(R_\sigma R_L C + L_\sigma) + R_\sigma + R_L}{sR_LC + 1},$$

$$\mathcal{L}[V_2] = \frac{V_1}{s}\,\frac{1}{L_\sigma C}\,\frac{1}{s^2 + s\left(\dfrac{R_\sigma}{L_\sigma} + \dfrac{1}{R_LC}\right) + \dfrac{1}{L_\sigma C}\left(1 + \dfrac{R_\sigma}{R_L}\right)}.$$

A slightly underdamped case was selected because the output pulse rises faster than for the critically or overdamped cases, and some oscillations in the output signal can, in general, be accepted. Hence,

$$V_2 = V_1\,\frac{R_L}{R_\sigma + R_L}\left[1 - e^{-\delta t}\left(\cos \omega_e t + \frac{\delta}{\omega_e}\sin \omega_e t\right)\right],$$

where:

$$\delta = \frac{1}{2}\left(\frac{R_\sigma}{L_\sigma} + \frac{1}{R_L C}\right), \quad \omega_0^2 = \frac{1}{L_\sigma C}\left(1 + \frac{R_\sigma}{R_L}\right),$$

$$\omega_c = \sqrt{\omega_0^2 - \delta^2}.$$

The rise time of the pulse can be defined by means of the critically damped case. The rise time is the time required for the pulse to rise from 0.1 to 0.9 of its final value. This rise time is[7]

$$t_r = 3.35\left[L_\sigma \frac{R_L}{R_\sigma + R_L} C\right]^{1/2}.$$

Using this formula, the maximum tolerable L_σ is found to be

$$L_\sigma = 180 \text{ nh},$$

with

$$t_r = 10 \text{ ns},$$

$$\frac{R_\sigma + R_L}{R_L} = 2,$$

$$C = 100 \text{ pf}.$$

Flat-Top Response

The performance of the transformer at the top of the pulse may be determined from the low-frequency equivalent circuit of Figure 3c.

$$\mathcal{L}[V_2] = \frac{V_1}{s} \frac{s R_L L}{s(R_\sigma L + R_L L) + R_\sigma R_L},$$

$$V_2 = V_1 \frac{R_L}{R_\sigma + R_L} \exp\left\{-\frac{R_\sigma R_L}{L(R_\sigma + R_L)} t\right\}.$$

This result could also easily be obtained without Laplace transformation by applying Thevenin's Theorem to the circuit shown in Figure 3c; thus, the equivalent circuit would be reduced to a resistor in series with an inductance, and V_1 would be replaced by V_1' where,

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[7] J. Millman and H. Taub, *Pulse and Digital Circuits*, Chap. 9, McGraw-Hill, 1956.

$$V_1' = \frac{R_L}{R_\sigma + R_L} V_1.$$

The maximum drop tolerated in a good pulse transformer is of the order of 10 per cent from the initial amplitude. Thus, the formula for V_2 can be rewritten by expanding the exponential function into a series in which only the linear term is significant. Hence,

$$V_2 = V_1 \frac{R_L}{R_\sigma + R_L} \left[1 - \frac{R_\sigma R_L}{L\,(R_\sigma + R_L)} t \right].$$

The top of the output pulse is tilted downward by

$$P = \left(\frac{R_\sigma R_L}{L\,(R_\sigma + R_L)} t_p \right) \times 100\%,$$

where t_p is the pulse width. Since $P = 10\%$ and $t_p = 30$ ns, L can be calculated;

$$L = \frac{10 \times 3 \times 10^{-8}}{.1} = 3\ \mu\text{h}.$$

Fall-Time Response

The applied source voltage at the input of the transformer goes to zero at the end of the pulse. This could also be interpreted as a negative-going pulse (same amplitude as positive pulse) applied to the input. The rise time and fall time of the output pulse of the transformer would be the same and, furthermore, the tail at the end of the pulse would decay with the same time constant as was found for the flat-top response, if all the circuit elements remained unchanged. This last assumption cannot be made in the case considered. The source impedance included in R_σ increases considerably at the end of the pulse and so does the load impedance because the conducting diode becomes back biased. The half-selected diodes contribute considerably to the capacitance C, and thus C also varies with the output voltage of the transformer.

The performance of the transformer at the trailing edge of the pulse may be calculated similarly to that of a ringing circuit.[7] The equivalent circuit considered is shown in Figure 5.

It is convenient to introduce Δ, the ratio of current in the inductor to current through the resistor R at the end of the pulse. Thus

$$\Delta = \frac{I}{V_0/R},$$

at $t = t_p$. The roots $p_{1,2}$ for the characteristic equation of the equivalent circuit in Figure 5 are

$$P_{1,2} = -\frac{1}{2RC} \pm \left[\left(\frac{1}{2RC}\right)^2 - \frac{1}{LC}\right]^{1/2}.$$

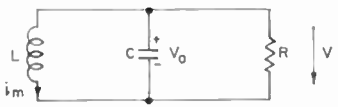


Fig. 5—Ringing circuit for calculating the fall-time response of the transformer.

In order to achieve a high repetition rate, the decay time for the pulse tail must be as short as possible. This means that a critically damped response curve should be obtained. The values of L and C cannot be changed, but R might be altered without interfering with the rise and flat-top response. At the end of the pulse, R increases considerably as was noted before. By shunting the secondary of the transformer with an additional resistor, a critically damped response characteristic may be obtained. The condition for critical damping is

$$\frac{1}{4R_k^2C^2} = \frac{1}{LC}.$$

Hence,

$$R_k = \frac{1}{2}\sqrt{\frac{L}{C}}.$$

With the values for L and C as used before,

$$R_k = 87 \text{ ohms}.$$

This 87 ohms does not change the response characteristic for the rise

and the flat top of the pulse appreciably, but improves the fall-time characteristic considerably. The latter can now be described by

$$\frac{V}{V_0} = \left[1 - (1 + 2\Delta)\frac{t}{\sqrt{LC}}\right] \exp\left\{-\frac{t}{\sqrt{LC}}\right\}.$$

A time constant τ can be defined

$$\tau = \sqrt{LC} = 17.3 \text{ ns}.$$

This time constant is sufficiently short for 100-ns cycle time operation.

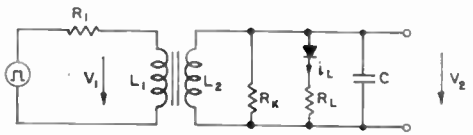
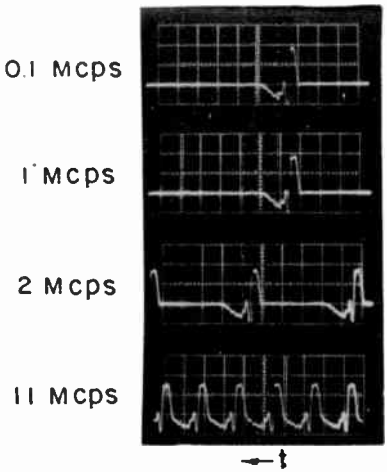


Fig. 6—Circuit to test transformer response with equivalent circuit of selected line as a load.

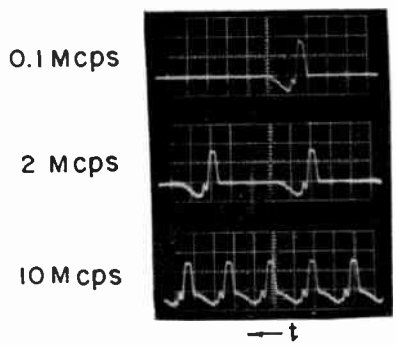
If the inductance L is reduced to 2 μh, the required value of R_k is 70 ohms, the drop $P = 13\%$, and the time constant $\tau = 14$ ns. Thus, very little is gained.

Several transformers were made according to the specifications given above and tested in the circuit shown in Figure 6. R_1 represents the source impedance of the transistor driver, L_1 and L_2 the primary and secondary inductances of the transformer (3 μh each), R_k an additional shunt resistance to minimize the decay time, and R_L the load impedance (10 ohms). The load current i_L was measured across R_L. Oscillographs are shown in Figure 7.

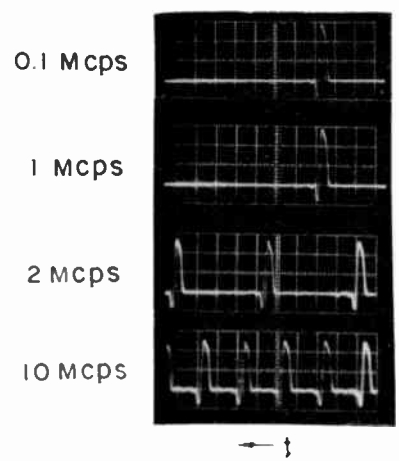
The rise and fall times of the voltage pulses at the primary and the secondary of the transformer are of the order of 10 ns, and the pulses are 30 ns wide at the base. The transformer has recovered 100 ns after the pulse started to rise; thus 100 ns cycle time operation is possible. Pulses of 500 ma peak current are obtained through the load resistor with 8 volts applied to the primary of the transformer. Rise and fall times of the load current are also of the order of 10 ns. The top of the current pulse is tilted upward due to conductivity modulation in the diode which reduces the total load impedance. The diode recovers within 10 ns after the pulse is turned off.



(a) Voltage V_1 on primary of transformer
50 ns/cm, 5v/cm



(b) Voltage V_2 at output of transformer
50 ns/cm, 5v/cm



(c) Current i_L
50 ns/cm, 200 ma/cm

Fig. 7—Oscilloscope tracings of measurements taken with the circuit shown in Figure 6.

Load-Sharing Switches Combined with a Bidirectional Diode Matrix

The number of outputs of a magnetic load-sharing switch is always smaller than the number of inputs.[5] The switch offers the advantage of adding the currents of several drivers into a given load. Neverthe-

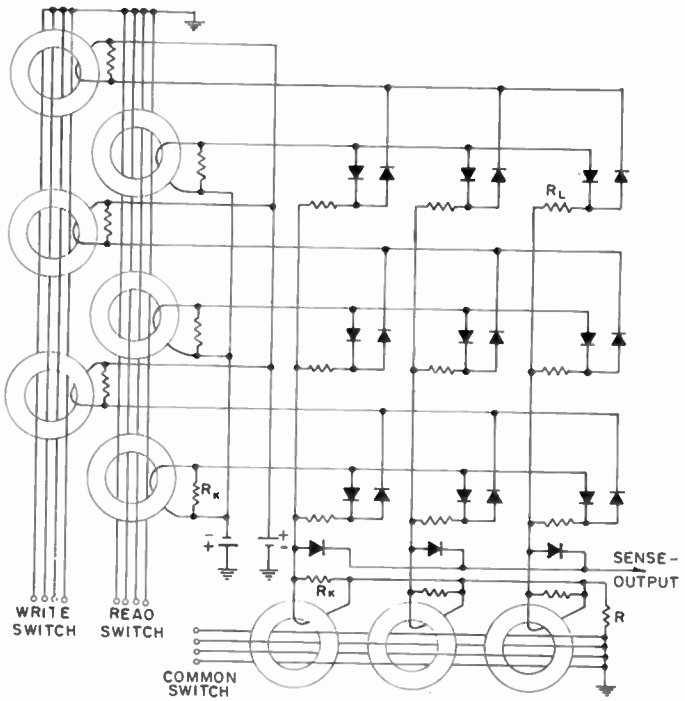


Fig. 8—Magnetic load-sharing switches driving a bidirectional diode matrix.

less, for a reasonably sized memory, the number of drivers required would be excessive. However, if it is possible to drive a rectangular diode matrix with load-sharing switches, the number of drivers may be greatly reduced. A rectangular bidirectional diode matrix with N loads requires 2 $\sqrt{N}$ bidirectional inputs. Normally, 4 $\sqrt{N}$ unipolar drivers are employed to drive a bidirectional diode matrix. A 3 × 3 bidirectional diode matrix driven by 3 load-sharing switches is shown in Figure 8. The loads R_L represent words or bits, depending on whether the memory is word or bit organized. Only 3 load-sharing switches are used since bidirectional output pulses can be generated

with unipolar drivers; thus, only one switch is needed for the common matrix lines. The switch cores may be considered to have recovered 100 ns after the leading edge of the applied pulse. Thus, the repetition frequency must be reduced to about 5 mc in order to insure proper operation. If separate wires for read and write pulses are used, then four switches must be used and the repetition frequency may be increased to 10 mc.

The matrix diodes are back biased with d-c voltage which is about equal in amplitude to the pulse amplitude at the secondary of the selected switch cores. In order to read from or write into a memory location, a core in the "common switch" and a core in the "read or write switch" must be energized. The total pulse amplitude (sum of common and, e.g., write pulse amplitudes) is less than or equal to twice V_0; thus only one diode in the entire diode matrix is forward biased during the time the pulses are applied, and all the other diodes carry either no current at all or only capacitive current if they are half selected.

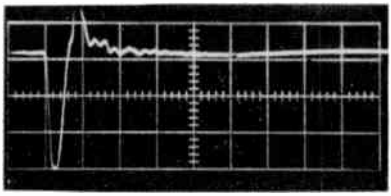
Results and Conclusions

An arrangement as shown in Figure 8 was built and tested. The memory is assumed to be bit organized to avoid additional electronics for the digit pulses. The loads R_L in Figure 8 are ferrite storage elements.

The current amplitudes used in the experiments do not actually require load-sharing switches since they may be delivered by single transistor drives, but this was a convenient setup for testing purposes.

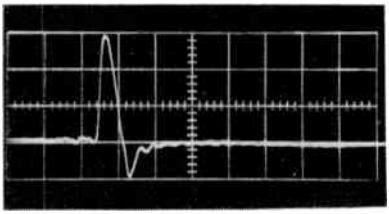
The cycle time for read–write pulses is 150 ns. Tests were made with values of V_0 ranging from 5 to 20 volts. The pulse amplitudes changed accordingly. The switching of the ferrite elements was observed by sensing through back-biased diodes connected to the common drive line. Oscilloscope photographs of the output pulses of the load-sharing switches and the sense signal are shown in Figure 9. The pictures were taken at a 1-mc repetition rate. For a cycle time of 150 ns, a 6-mc repetition rate should be possible. The repetition rate was increased to 6 mc, and it was found that the load current amplitudes decreased by about 50%, while the output voltages of all three switches increased slightly (Figure 10). Careful inspection of the circuitry revealed that the bias supplies for the diodes are responsible for the current reduction.

The supplies were shunted with resistors to reduce the time constants involved. Figure 11 shows the load current pulses at 7 mc. The pulse amplitudes are reduced by about 10% due to the repetition rate



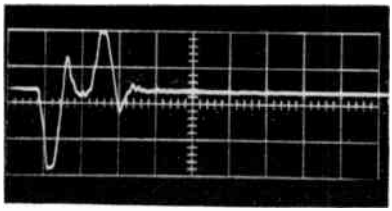
→ t

(a) Read pulse
50 ns/cm, 5 v/cm



→ t

(b) Write pulse
50 ns/cm, 5 v/cm



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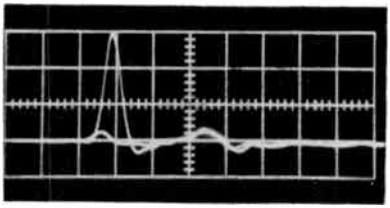
(c) Load current
50 ns/cm, 100 ma/cm

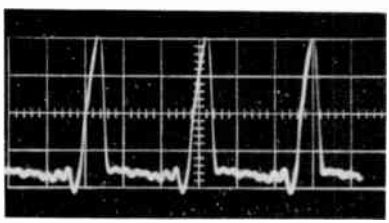


→ t

(d) Sense voltage
10 ns/cm, 0.1 v/cm

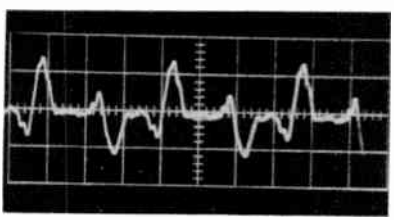
Fig. 9—Output pulses, load current and sense signal at 1 mc repetition rate.

increase from 1 to 7 mc. It is concluded that these load sharing switches and the diode matrix may be operated at 6 mc. This upper limit is due to the common switch, and the use of two separate switches instead of a common one permits operation at a 10-mc repetition rate. It is also possible to use only two load-sharing switches instead of three. The read and write switches are combined into one switch with two output lines for each core. Bidirectionality in this case is achieved



← t

(a) Read pulse
50 ns/cm, 5 v/cm



← t

(b) Load current
50 ns/cm, 100 ma/cm

Fig. 10—Output pulse and load current amplitudes at 6 mc.

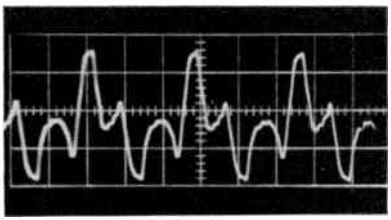


Fig. 11—Load current at 7 mc (50 ns/cm, 100 ma/cm).

as mentioned earlier. Operation at 5 to 6 mc repetition rate might well be achieved with this configuration.

The tests indicate the feasibility of high-speed magnetic load-sharing switches combined with diode matrices. Special care must be taken, however, that all the pulses applied to the switches are in proper coincidence and stray capacitances must be kept small.

ACKNOWLEDGMENT

The author gratefully acknowledges the encouragement given to him by J. A. Rajchman and the stimulating discussions with R. Shahbender.

series resistance. Penfield and Rafuse[8] have made a detailed analysis of harmonic generation with diodes having internal losses, and have shown that the conversion efficiency is closely related to the maximum cutoff frequency of the device. This maximum cutoff frequency, f_{cm}, is given by

$$f_{cm} = \frac{1}{2\pi R\, C_{\min}}, \tag{1}$$

where $C_{\min}$ is the junction capacitance at breakdown voltage and R is the diode series resistance.

The conversion efficiency, η, can, for high efficiencies, be approximated as follows:

$$\eta = 1 - D\frac{f_{in}}{f_{cm}} \tag{2}$$

when $f_{cm}/f_{in} > 100$. f_{in} is the fundamental frequency and D is a constant equal to 20.8 for an abrupt-junction doubler, 34.8 for a tripler, 62.5 for a quadrupler, and 92.9 for a quintupler. (These values are based on theoretical efficiencies computed for many operating conditions.[7])

The analyses which have been made of harmonic generation assume the series resistance of the diode to be a constant independent of applied voltage. Although this assumption is approximately true for low-voltage diodes, it is not valid (as will be shown later) for high-voltage epitaxial structures designed for optimum cutoff frequency. The equations given above, therefore, are only rough approximations for these diodes, and defining a figure of merit for such a device becomes difficult.

Power-Handling Capability

The maximum power, P_{in}, stored at any instant by a lossless linear capacitor is given by

$$P_{in} = \frac{1}{2}\omega_{in} CV^2, \tag{3}$$

where $2V$ is the amplitude of the sinusoidal wave, $\omega_{in} = 2\pi f_{in}$, and C is the capacitance. In a variable-capacitance diode, the maximum input

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[8] P. Penfield and R. P. Rafuse, *Varactor Applications*, The M.I.T. Press, 1962.

power depends on the way in which the diode is operated, but the form of the expression is similar to that given above;

$$P_{in} = B\omega_{in} C_{min} V_B^2 \tag{4}$$

where B is a constant which depends on the order of harmonic desired, C_{min} is the minimum junction capacitance, and V_B is the diode breakdown voltage. Experimental values of B have been found to vary between 1 and 1/30. Large values are possible at low frequencies if use is made of the large diffusion capacitance which results from minority-carrier storage when the diode is forward-biased.

It would appear that high breakdown voltages and/or high capacitance values may be equally acceptable to achieve large power-handling capacitance in high-frequency circuits. Frequently, however, it is desirable to limit the junction capacitance in high-frequency circuits. High breakdown voltages are therefore essential for large power input in such circuits, and the upper limit to the diode power input may be determined, not by its electrical parameters, but rather by its thermal characteristics. An increase in electrical power-handling capability is accompanied by an increase in the thermal dissipation of the device, because the power dissipated in the series resistance also increases.

The maximum allowable thermal power dissipation, $P_{diss}(\max)$, is determined by the maximum permissible junction-temperature rise above the ambient temperature (determined by the semiconductor) and the thermal resistance, R_{th}, as follows:

$$P_{diss}(\max) = \frac{T_j(\max) - T_0}{R_{th}} \tag{5}$$

where $T_j(\max)$ is the maximum junction temperature and T_0 is the ambient temperature.

High conversion efficiency, low thermal resistance, and high maximum operating junction temperatures are therefore important parameters for harmonic-generator diodes.

Diode Structure and Design Theory

In this section, diode parameters and their relationship to the device structure for different semiconductors are analyzed in detail for a step-junction model.

Cutoff Frequency

Figure 1 shows the assumed diode impurity profile. The following assumptions are made in the subsequent calculations:

(a) The p+n junction is abrupt. In silicon this assumption is a reasonably good approximation for shallow diffused junctions having high surface concentrations. The impurity profile for zinc layers diffused into gallium arsenide at temperatures in excess of 1000°C is such that nearly abrupt junctions result.[9,10]

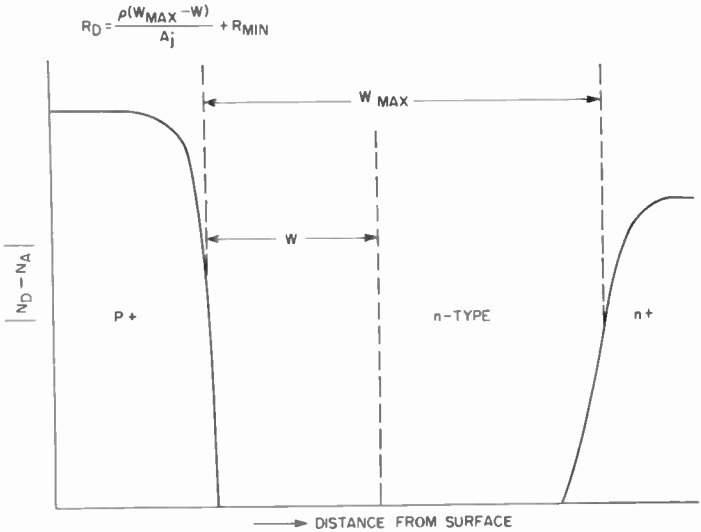

Fig. 1—Assumed device profile.

(b) The nn+ interface is abrupt, and the doping of the n-region is uniform. Most vapor-deposited layers do, in fact, have a small built-in impurity gradient, and the net impurity concentration is a function of the distance from the n+ substrate.

(c) The spreading effect of resistance is neglected. This assumption is reasonably correct if the diameter of the diode is several times larger than the thickness of the high-resistivity n-type layer.

(d) The series resistance of the diode is concentrated in the region between the edge of the junction depletion region and the n+

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[9] B. Goldstein, "Diffusion of Cadmium and Zinc in Gallium Arsenide," *Phys. Rev.*, Vol. 118, p. 1024, May 1960.

[10] F. A. Cunnel and C. H. Gooch, "Diffusion of Zinc in Gallium Arsenide," *Jour. Phys. and Chem. Solids*, Vol. 15, p. 127, Aug. 1960.

layer. This assumption is valid for thin, highly doped p^+ and n^+ regions at frequencies where the skin effect may be neglected.

As mentioned previously, the theoretical work relating device parameters to circuit performance was based on the assumption that the diode series resistance is a constant independent of the applied bias. The resulting expression for conversion efficiency (Equation (2)) is given in terms of the maximum cutoff frequency (at the breakdown voltage). If, however, the resistance is actually higher at lower bias points, the internal diode losses are higher than the predicted values and, as a result, the conversion efficiency is lower than the values predicted by the theory. It is difficult to define an average resistance because such a value depends on the way in which the diode is used. It is of interest, therefore, to consider the cutoff frequency at a low bias point, where the resistance is very nearly at its maximum value, and to compare silicon and GaAs p^+nn^+ devices.

The minimum n-type layer thickness required is equal to the width of the junction depletion region at breakdown, W_{max}. The resistivity should, of course, be such that the desired breakdown voltage is attained.

The width of the depletion region, W, at a given applied voltage is

$$W = \sqrt{2\epsilon\rho\mu(V - \phi)} \tag{6}$$

where ρ is the resistivity of the lightly doped side of the junction, μ is the electron mobility for the p^+n junction, V is the applied voltage, ϕ is the junction potential (1 volt for GaAs, 0.7 volt for silicon), and ϵ is the permittivity. The minimum n-type layer thickness, W_{max}, is given by

$$W_{max} = \sqrt{2\epsilon\rho\mu(V_B - \phi)}. \tag{7}$$

The diode resistance at zero applied voltage, $R_D(\max)$, is given by

$$R_D(\max) = \frac{\rho W_{max}}{A_j}, \tag{8}$$

where A_j is the junction area. The resistance R_D at any bias voltage V is given by

$$R_D = R_D(\max) - \frac{\rho W}{A_j}, \tag{9a}$$

or

$$R_D = \left[\frac{2\rho^3\epsilon\mu}{A_j^2}\right]^{1/2} [(V_B - \phi)^{1/2} - (V - \phi)^{1/2}], \tag{9b}$$

where the value of C_V is given by

$$C_V = A_j\left[\frac{2\rho\mu(V-\phi)}{\epsilon}\right]^{-1/2}. \tag{10}$$

The cutoff frequency, f_c, at low bias values can be determined by combining Equations (9) and (10);

$$f_c \cong \frac{1}{2\pi R_D(\max)\, C_V}, \tag{10a}$$

or

$$f_c \cong \frac{1}{2\pi\rho\epsilon}\left(\frac{V-\phi}{V_B}\right)^{1/2}, \tag{10b}$$

when $V_B \gg V - \phi$.

Contact resistances, the resistance of the n+ region, and other resistances that are present at microwave frequencies cannot in practice be neglected. They are, however, difficult to predict analytically. The lowest resistance measured at 2 gigacycles was about 0.5 ohm. A minimum of 1 ohm at X-band is probably not unreasonable. If these additional resistances are lumped under a total value $R_{\min}$, the actual cutoff frequency f_{ca} which can be expected is given by

$$\frac{1}{f_{ca}} = \frac{1}{f_c} + \frac{1}{f_{cm}}, \tag{11}$$

where

$$f_{cm} = \frac{1}{2\pi R_{\min} C_V}.$$

Equation (10b) shows that the lower the resistivity required to achieve a given value of breakdown voltage, the higher the cutoff frequency. Figure 2 shows breakdown voltage as a function of resistivity for silicon and gallium arsenide p+n junctions. (Germanium is not considered because its low maximum operating temperature severely limits permissible thermal dissipation.)

As a result of the higher electron mobility and larger band gap of

gallium arsenide, the breakdown voltages of the gallium arsenide diodes are higher than those of the silicon devices when materials of equal resistivity are used. Breakdown voltage and resistivity are shown as a function of carrier concentration in Figures 3 and 4, respectively. The curve for silicon in Figure 3 is based on a composite plot of Irvin.[11] The minimum energy which an electron must possess to produce an electron–hole pair is in excess of the band gap. Because the band gap

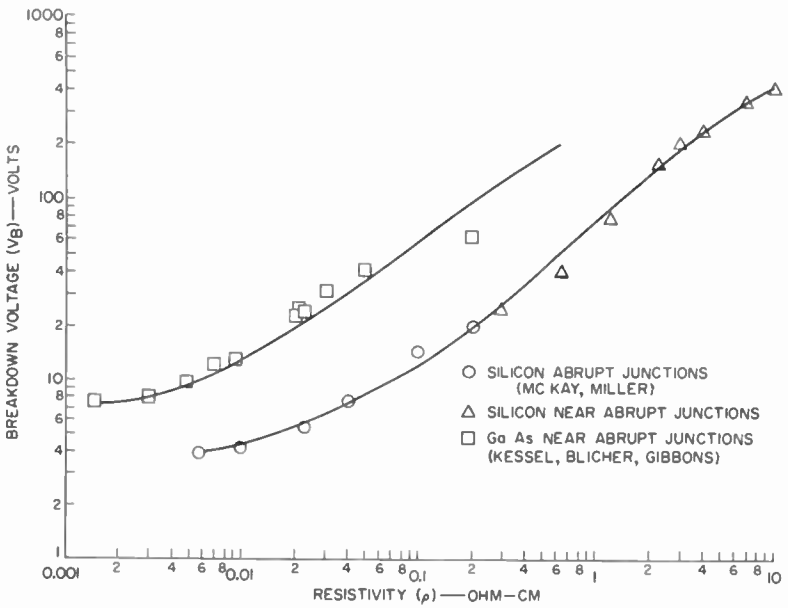

Fig. 2—Breakdown voltage V_B as a function of resistivity ρ of the n-type side of silicon and GaAs p+n junctions.[12–15]

of gallium arsenide is greater than that of silicon, the electric field in the depletion region must be higher before avalanche breakdown occurs.

Equation (10b) is plotted in Figure 5. The theoretical maximum cutoff frequency f_{cm} at a total junction potential of 2 volts is shown

[11] J. C. Irvin, "Resistivity of Bulk Silicon and of Diffused Layers in Silicon," *Bell Syst. Tech. Jour.*, Vol. 41, p. 387, March 1962.

[12] K. G. McKay, "Avalanche Breakdown in Silicon," *Phys. Rev.*, Vol. 94, p. 877, May 1954.

[13] S. L. Miller, "Ionization Rates for Holes and Electrons in Silicon," *Phys. Rev.*, Vol. 105, p. 1246, Feb. 1957.

[14] H. Kressel, unpublished data. These diodes consist of very shallow (1μ) highly doped boron-diffused junctions.

[15] H. Kressel, A. Blicher, and L. H. Gibbons, Jr., "Breakdown Voltage of GaAs Diodes Having Nearly Abrupt Junctions," *Proc. I.R.E.*, Vol. 50. p. 2493, Dec. 1962. (The GaAs curve is drawn somewhat differently in the present paper.)

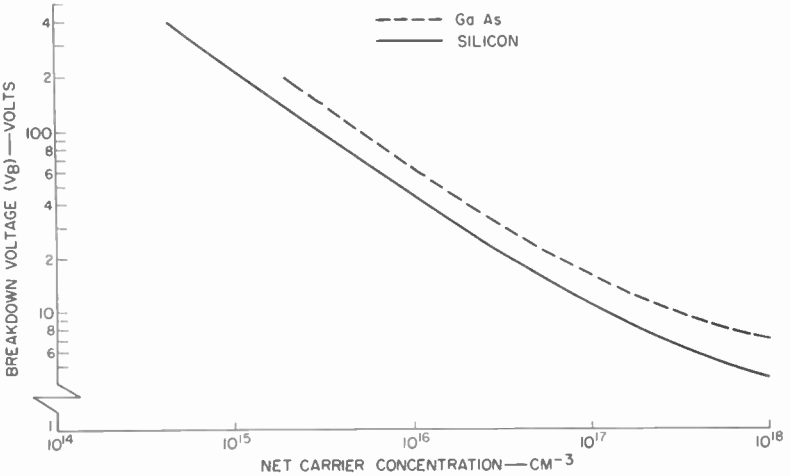

Fig. 3—Breakdown voltage V_B as a function of net carrier concentration in the n-type base of p+n GaAs and silicon diodes.

for p+nn+ gallium arsenide and silicon diodes as a function of breakdown voltage. These curves are based on the experimental relationship between ρ and V_B shown in Figure 2.

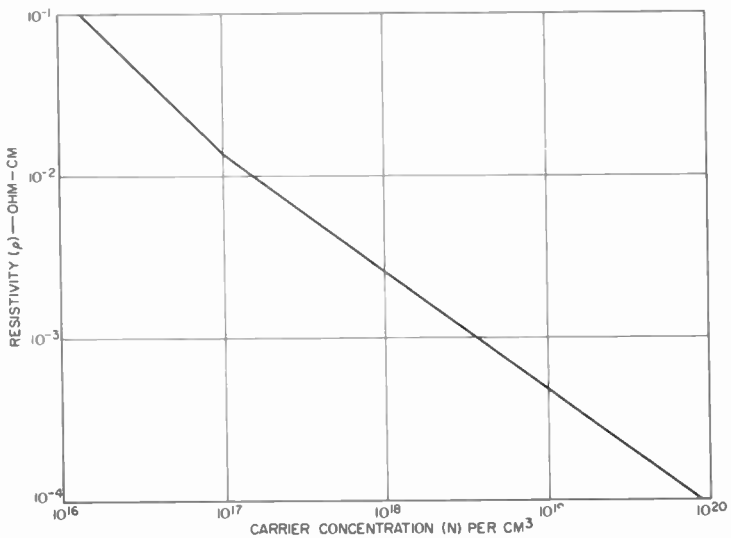

Fig. 4—Resistivity as a function of carrier concentration for n-type GaAs.[16]

[16] J. Hilibrand, Private Communication.

The maximum cutoff frequencies shown in Figure 5 may be exceeded in practice if the mobilities of the particular crystal used are greater than the values used in the calculations. The frequency limits are assumed to be independent of junction areas. As the junction capacitance is increased, however, Equation (11) shows that the measured value of cutoff frequency will tend to decrease because R_{min} is relatively constant. The highest-cutoff diodes, therefore, are most

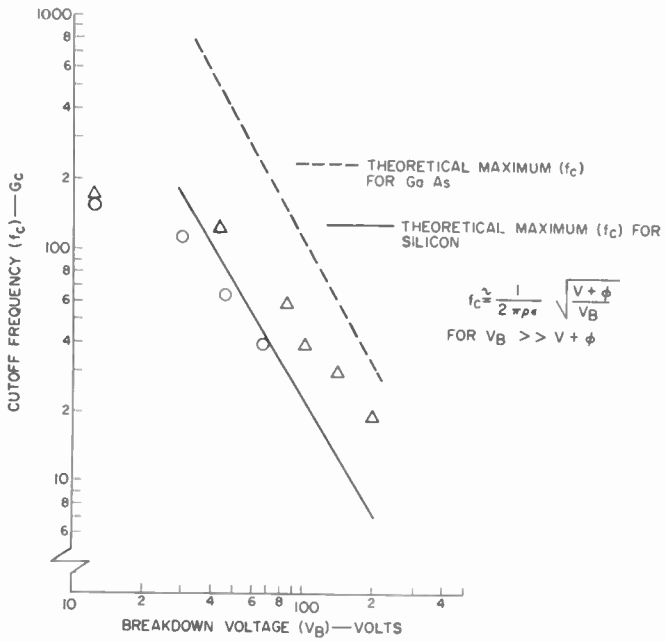

Fig. 5—Theoretical maximum cutoff frequency (f_{cm}) at $V - \phi = 2$ volts for GaAs and silicon abrupt-junction diodes as a function of breakdown voltage (V_B). The experimental points show representative epitaxial (△) and non-epitaxial (O) GaAs diodes (intermediate between graded and abrupt junctions).

likely to be produced when the junction capacitance is small and R_{min} is a small part of the total resistance.

It is evident that superior diodes can theoretically be obtained by use of gallium arsenide, provided comparable breakdown voltages can be achieved in both materials.

Equation (9b) indicates that the semiconductor resistance approaches zero when the applied voltage is such that the depletion region reaches the n^+ substrate. For a properly designed diode, this effect occurs at the breakdown voltage; the cutoff frequency at this point is then independent of the particular value of the diode breakdown

voltage. As the breakdown voltage increases, however, the resistance change between zero bias and breakdown becomes increasingly large. It is of interest to compare this resistance change as a function of breakdown voltage for gallium arsenide and silicon diodes having the same area. The expression $(R_D(\max) + R_{\min})/R_{\min}$ is plotted in Figure 6 for gallium arsenide and silicon diodes having an area of 3.23×10^{-3}

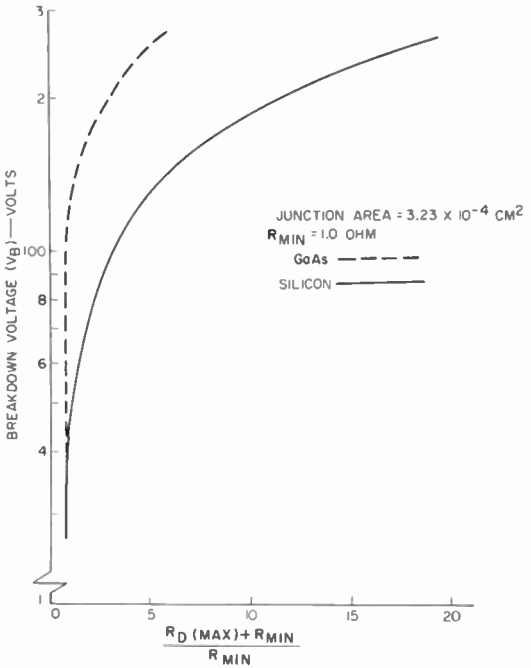

Fig. 6—Theoretical $(R_D(\max) + R_{\min})/R_{\min}$ for abrupt GaAs and silicon p+nn+ diodes having a junction area of 3.23×10^{-3} cm^2.

square centimeter and a resistance $R_{\min}$ of 0.5 and 1 ohm, respectively. Diodes having breakdown voltages of less than 100 volts show small resistance changes, but the effect becomes appreciable in diodes having breakdowns greater than 150 volts. The resistance changes become more noticeable in small junctions, where the resistance in the n-type region is appreciable compared to $R_{\min}$. Figure 7 shows curves similar to those of Figure 6 for a junction ten times smaller.

Thermal Considerations

The thermal resistance of the diode is determined by the junction

area, the base thickness, the semiconductor thermal conductivity, and the package design.

If the junction diameter is several times larger than the base thickness, spreading effects can be neglected; the junction-to-base thermal

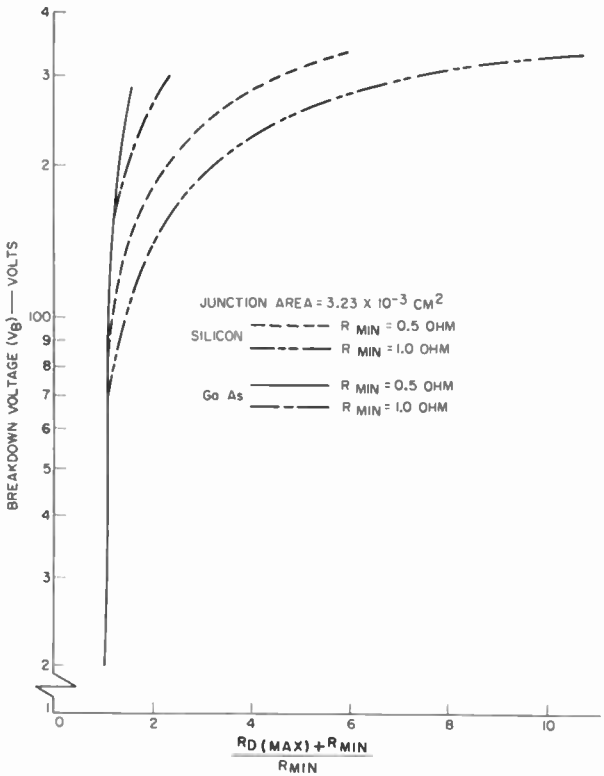

Fig. 7—Theoretical $(R_D(\max) + R_{min})/R_{min}$ for abrupt junction GaAs and silicon p+nn+ diodes having a junction area of 3.23×10^{-4} cm².

resistance R_{th} is then given by

$$R_{th} = \frac{t}{\pi R_j^2 \sigma_{th}}, \tag{12}$$

where σ_{th} is the thermal conductivity (0.5 watt/cm-°C for gallium arsenide, 0.84 watt/cm-°C for silicon), t is the diode base thickness, and R_j is the junction radius.

Because gallium arsenide is less brittle than silicon, pellets less

than 70 microns thick can be readily fabricated, and t can be as low as 0.005 centimeter. Silicon wafers must generally be about twice as thick to avoid excessive processing losses. For a given junction area, therefore, the thermal resistance of gallium arsenide and silicon devices can be essentially the same in spite of the lower thermal conductivity of gallium arsenide. For small junctions, where spreading effects cannot be neglected, the thermal resistance may be calculated by use of the solutions of the Laplace equation given by D. P. Kennedy.[17] The maximum junction operating temperature is determined by the maximum allowable saturation current, which is a function of the semiconductor band gap. High values of saturation current reduce the effective cutoff frequency of the diode because the shunt circuit path established results in an apparent increase in the diode resistance. As a result, the conversion efficiency may be substantially decreased. As shown in Table I, the maximum operating temperature is about 175°C for silicon, 100°C for germanium, and 300°C for gallium arsenide. The actual maximum operating temperature of the gallium arsenide microwave diodes described in this paper is presently limited to about 220°C by the materials used to make ohmic contacts to the junction.

The thermal figure-of-merit ratio for the thermal power dissipation of gallium arsenide and silicon diodes of identical construction is, therefore, given by

$$\frac{\Delta T(\text{GaAs})}{\Delta T(\text{Si})} = \frac{220°\text{C} - 25°\text{C}}{175°\text{C} - 25°\text{C}} = 1.3 \qquad (13)$$

where $\Delta T(\text{GaAs})$ and $\Delta T(\text{Si})$ represent the allowable junction-temperature rise above ambient for gallium arsenide and silicon, respectively. The value of Equation (13) could potentially be greater than 2. The package thermal resistance may be minimized by keeping the path between the pellet and heat sink as short as possible and by the use of high-thermal-conductivity materials.

Materials

Single-crystal layers of gallium arsenide were grown from the vapor phase on low-resistivity silicon-doped substrates. An open-tube process in which gallium arsenide is synthesized chemically was used.

[17] B. P. Kennedy, "Spreading Resistance in Cylindrical Semiconductor Devices," *Jour. Appl. Phys.*, Vol. 31, p. 1490, Aug. 1960.

Gallium trichloride (or HCl) was reacted with gallium metal, and the products of the reaction were combined with arsenic to form gallium arsenide. Both the gallium and the arsenic were the highest-purity grades available commercially. Hydrogen, used as a carrier gas and to provide a reducing atmosphere, was obtained from a palladium diffuser. Layer thickness was varied from 10 to 25 microns, as determined by both angle-lapping and infrared-interference techniques. Surfaces of all layers were generally smooth.

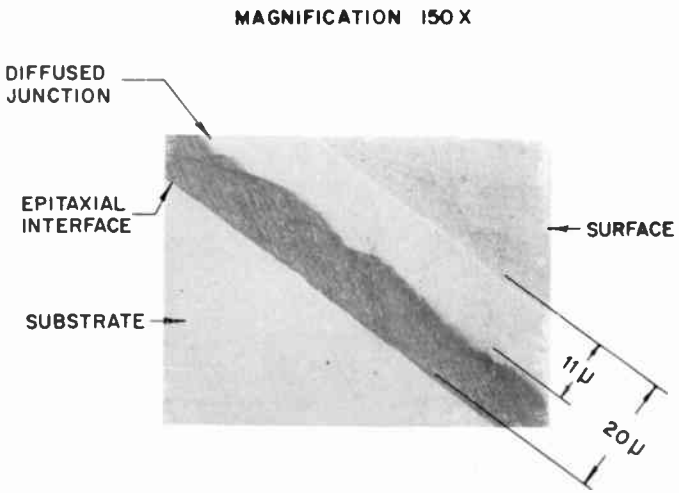

Fig. 8—Cross-section of a zinc diffused epitaxial layer.

Device Fabrication

Diffusion is accomplished in a sealed quartz ampoule. A sufficient amount of zinc is introduced to maintain a high zinc concentration during diffusion. The typical junction depth is about 8 microns. A solution of copper sulfate is used to delineate the junction. The nn^+ interface is also clearly delineated so that the thickness of the p^+ and n regions after diffusion can readily be measured, as shown in Figure 8.

Thermal conversion of n-type material to near-intrinsic or even p-type material, which is frequently observed when high-resistivity melt-grown gallium arsenide is diffused at high temperature, does not seem to occur as readily for high-resistivity vapor-deposited layers. Layers having carrier concentrations below 10^{15} carriers per cubic centimeter have been successfully diffused at 1000°C. More experimental data is required, however, before any conclusions can be drawn.

After diffusion, the slices are lapped, cut apart, and soldered into the ceramic package. A sphere of suitable composition to form the contact to the p side of the junction is then alloyed on the diffused p layer. A fine screen is subsequently soldered to both the p-contact dot and the top of the package. The junction is defined by electrolytic etching, the alloyed sphere acting as a mask. This technique permits close control of the junction capacitance. The device is then thoroughly rinsed in deionized water, baked in dry nitrogen, and hermetically

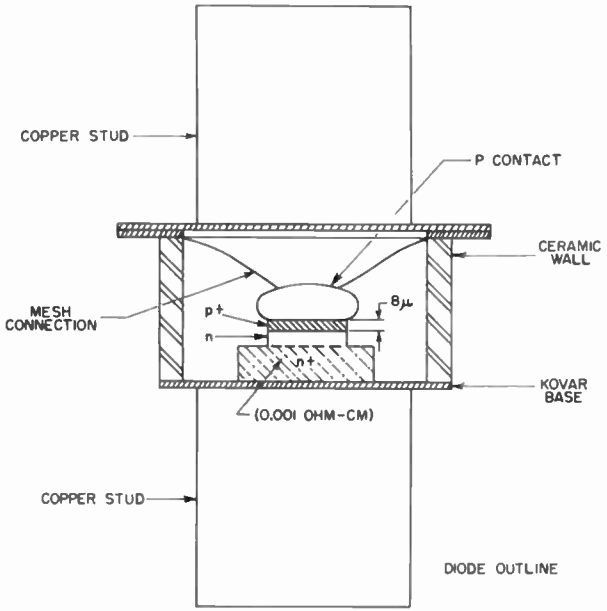

Fig. 9—Complete diode outline.

sealed in a dry box by welding a cap to the rim on the base of the package. Figure 9 shows the completed unit. The package inductance is typically 0.4 nanohenry and the package capacitance is about 0.3 picofarad.

Experimental Results

Diodes having breakdown voltages between 8 and 240 volts have been fabricated on epitaxial n-type layers. Most of the units fabricated have been small-area devices. The use of small areas permits better evaluation of the inherent diode quality because the semiconductor resistance is much larger than R_{min}. Typical junction capacitances

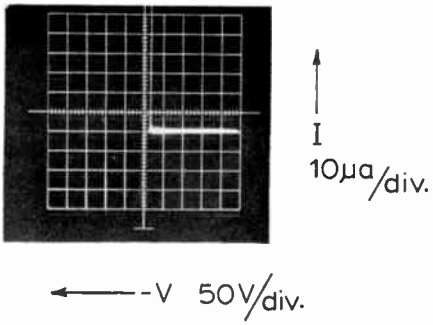

Fig. 10—Typical reverse current–voltage curve for a high-voltage epitaxial GaAs diode.

at zero bias ranged from 0.5 to 2.0 picofarads (measured at 1 megacycle). The reverse current is very small (less than 0.01 microampere at one half the breakdown voltage), and the knee at breakdown is typically sharp, as shown in Figure 10. The capacitance–voltage curve indicates that the junction profile is intermediate between an abrupt and a graded one. Figure 11 shows capacitance as a function of voltage for a typical epitaxial 200-volt diode and for a similar device fabricated on a graded epitaxial layer.

Control of the layer thickness and resistivity is critical in the determination of the device characteristics. If the epitaxial layer is too thin for a given value of resistivity, the edge of the depletion region reaches the substrate prior to the breakdown voltage, and the capacitance ceases to change after that point. Further complications are

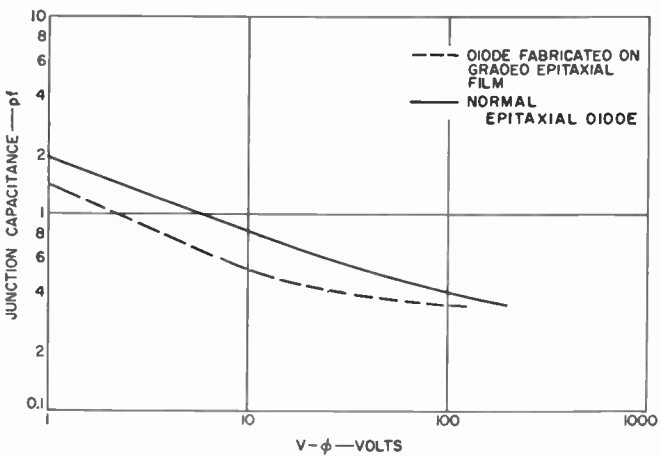

Fig. 11—Capacitance–voltage curves for a normal epitaxial diode and for a diode fabricated on a graded epitaxial film.

introduced by the doping gradient observed in many high-resistivity layers. With a large gradient, the exponent of the capacitance–voltage equation of junctions changes from 0.45 at low values of applied bias, to 0.33 at higher voltages, and to about 0.2 at still higher voltages.

Representative experimental values of cutoff frequency for epitaxial high-voltage diodes are shown in Figure 5. The measurements were made at 10.2 gigacycles by means of Houlding's technique.[18] Results for devices fabricated on melt-grown gallium arsenide are also shown. The epitaxial gallium arsenide devices are superior to the theoretical maximums for silicon, while the nonepitaxial diodes are approximately equivalent to the silicon maximum values. As expected, the experimental results were lower than the computed maximum values of cutoff frequency. There are several possible reasons for this discrepancy, the major one being the difficulty of controlling the thickness of the high-resistivity region to the tolerances required to achieve optimum results. The actual layer thicknesses are in general greater than required. In addition, surface and crystal imperfections may cause breakdown to occur at voltages lower than those shown in Figure 2. Other resistances, mentioned earlier, further reduce the measured cutoff-frequency values. The devices described are able to dissipate a maximum of 1 watt; the higher-voltage diodes would be thermal-dissipation-limited if operated at sufficiently high frequencies.

An obvious extension of this work is the fabrication of larger-area devices having better thermal characteristics. The cutoff frequencies for such devices, however, can be expected to be somewhat lower than those described.

Conclusion

Gallium arsenide epitaxial diodes promise to yield devices having cutoff-frequency values substantially higher than those of comparable-voltage silicon diodes. The implications of these results are important in that efficient harmonic-generator circuits handling several watts of power at frequencies up to X-band will become practical.

Acknowledgments

The authors thank A. Blicher and F. L. Vogel, Jr., for their helpful suggestions; H. C. Lee, M. A. Klein, and A. H. Solomon for numerous measurements; and G. Kupsky and A. G. Frey for assistance in the fabrication of the devices.

[18] N. Houlding, "Measurement of Varactor Quality," *Microwave Jour.*, Vol. 3, p. 40, Jan. 1960.

HIGH-CUTOFF-FREQUENCY GaAs DIFFUSED-JUNCTION VARACTOR DIODES*

By

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Summary—A gallium arsenide small-area diffused-junction varactor diode for use in the microwave frequency range is described. Typical cutoff frequency values obtained are in the neighborhood of 200 gigacycles at —6 volts. The properties of gallium arsenide are compared with those of germanium and silicon to show the advantages offered by gallium arsenide in varactor performance. The figures of merit of paramount importance in parametric amplifiers are discussed, as well as compromises which were made to achieve highest performance in X-band amplifiers. Typical characteristics are presented. Finally, the performance of these diodes in X-band nondegenerate parametric amplifiers is discussed.

Introduction

SEMICONDUCTOR VARIABLE-CAPACITANCE DIODES have become increasingly important in many applications, particularly for parametric amplification and for harmonic and subharmonic generation. Although varactor diodes with satisfactory characteristics have been available for frequency ranges approaching the microwave region, the lack of suitable diodes for higher frequencies has hampered efforts to seek out new (higher) frequency bands for communication media.

This paper describes a small-area diffused-junction gallium arsenide varactor diode designed for use in low-noise microwave parametric amplifiers. Because the desirable qualities of varactor diodes for this application had not been determined uniquely at the beginning of the development, the performance of this gallium-arsenide device in microwave parametric amplifiers was evaluated throughout the program. Results of this study are included because the data obtained were useful in achieving optimum design and characteristics of the diode.

Crystalline Material

The first consideration in the design of a microwave-frequency

* A portion of this work was performed under the sponsorship of the Electronic Technology Laboratory, Aeronautical Systems Division, Air Force Systems Command, United States Air Force.

varactor diode is the selection of the semiconductor material. Table I lists the important design parameters of the three materials considered: germanium, silicon, and gallium arsenide. Germanium is usually considered more suitable than silicon for high-frequency devices on the basis of carrier-mobility values. This difference is partially compensated by the lower dielectric constant of silicon, its higher dielectric breakdown (and resulting higher junction-breakdown voltages for comparable doping), and its higher band-gap value, which permits higher-temperature operation and greater power dissipation for comparable mesa areas.

Table I—Important Design Parameters of Semiconductor Materials for Varactor Diodes

Property	Ge	Si	GaAs
Band Gap (25°C)	0.68	1.11	1.40
Dielectric Constant	15.7	11.7	11.1
Electron Mobility ($N_D = 10^{17}$ cm^{-3})	2200	600	4500
Hole Mobility ($N_A = 10^{17}$ cm^{-3})	1000	220	220
Junction Built-in Potential (volts)	~0.4	~0.7	~1.0

Gallium arsenide appears most suitable for high-frequency, high-temperature, and high-power devices, however, because it combines the desirable features of both germanium and silicon. Figure 1 compares the carrier mobilities of the three materials. Because the cutoff frequency for a given breakdown voltage is proportional to carrier mobility, gallium-arsenide diodes can be expected to have a higher cutoff frequency than either germanium or silicon diodes (for equivalent breakdown voltages).

Varactor-Diode Equivalent Circuit

The junction of the diode shown in Figure 2 is constructed by means of solid-state impurity diffusion into a substrate. The mechanical stability of the mesa varactor structure shown is inherently superior to that of point-contact structures because the mesa contact is not merely a pressure contact, but is alloyed into the diffused layer.

The equivalent circuit shown in Figure 3 includes the electrical parameters of both the junction and the package. The package capacitance C_p and inductance L_p are assumed to be constant; these lossless

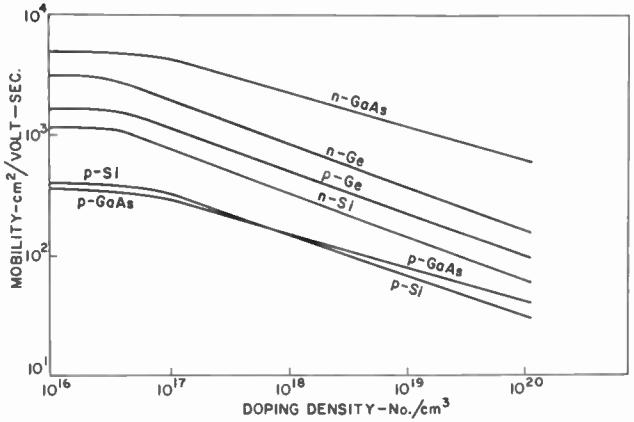

Fig. 1—Variation of mobility with impurity concentration.

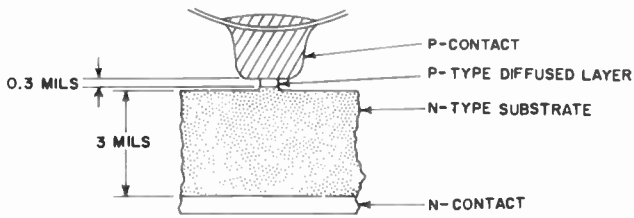

Fig. 2—Mesa structure of GaAs varactor diode.

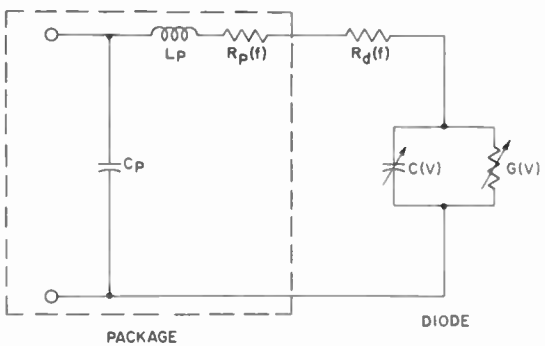

Fig. 3—Varactor diode equivalent circuit.

elements are not considered in the evaluation of the diode. The package dissipative resistance R_p is negligible at low frequencies, but becomes appreciable in the microwave-frequency range and can severely limit performance if it becomes excessively high. This resistance can be minimized by the use of a high-conductivity metallic layer on all metal parts of the package.

The diode series resistance $R_d(f)$ is the sum of the resistances of the semiconductor material on both sides of the junction and the contact resistances. Although $R_d(f)$ decreases slightly at elevated temperatures, it is assumed to be constant over the temperature range considered. Therefore the total series dissipative resistance, $R_s(f)$, is the sum of the package and diode resistances, as follows:

$$R_s(f) = R_p(f) + R_d(f). \tag{1}$$

The equivalent circuit of the diode itself is represented by the resistance $R_d(f)$ in series with the parallel arrangement of the junction capacitance $C(V)$ and the junction shunting conductance G (V). A high-performance diode in the microwave-frequency range generally must have a junction capacitance $C(V)$ of the order of one picofarad or less. The junction current through the shunting conductance $G(V)$ is negligible in the reverse-bias region, and is small over the dynamic range employed as compared to the component of current through the capacitance in the microwave frequency region. The equivalent circuit of the diode alone can thus be considered as a series resistive–capacitive circuit.

Varactor-Diode Figures of Merit

Several figures of merit for predicting diode performance in parametric amplifiers have been evolved. The quality factor Q for a particular bias point and frequency is defined as

$$Q(V,f) = \frac{1}{2\pi f R_s(f) C(V)}. \tag{2}$$

Q is a function of frequency both explicitly and through the total series resistance $R_s(f)$; it is a function of voltage through the junction capacitance $C(V)$ at the bias point.

An alternative figure of merit which may be derived from Equation (2) is the frequency for which Q is unity, or the cutoff frequency at the bias point. This frequency, f_{co}, is defined as

$$f_{co}(V,f) = \frac{1}{2\pi R_s(f)C(V)}. \tag{3}$$

There is no generally accepted voltage at which Q and f_{co} are evaluated. Uhlir[1] has suggested that the bias point at which $C(V)$ is a minimum be used (i.e., the reverse breakdown voltage). In the evaluations reported in this paper, the more conservative points of —1 and —6 volts are used.

A third figure of merit is the exponent n used in the following junction capacitance–voltage expression:[2]

$$C(V) = \frac{K}{(\phi_0 - V)^n}, \tag{4}$$

where K is independent of voltage and ϕ_0 is the built-in junction voltage. The value of ϕ_0 is approximately one volt for the gallium-arsenide diodes discussed in this paper. The constant K depends on the dielectric constant of the semiconductor material employed, the impurity concentrations, and the type of junction. The value of n is approximately 1/2 for abrupt junctions and 1/3 for graded junctions; larger values of n tend to improve performance of a parametric amplifier.

A fourth figure of merit is the capacitance ratio $\Delta C/C$, which is defined as follows:

$$\frac{\Delta C}{C} = \frac{C_{-1} - C_{-6}}{C_{-1}}. \tag{5}$$

This quantity is easily measured and provides a convenient indication of junction characteristics in terms of a circuit parameter. Equation (4) shows that the ratio $\Delta C/C$ is a function of both n and ϕ_0 at zero bias; there is a marked dependence on n, but relatively little on ϕ_0. Table II lists values of $\Delta C/C$ calculated for gallium arsenide abrupt and graded junctions for ϕ_0 values of 0.9, 1.0, and 1.1 volts.

Other parameters which should be considered in the evaluation of a varactor diode include reverse breakdown voltage, reverse leakage current, and the magnitude of the junction capacitance. The breakdown voltage must be large enough so that the diode can accommodate the peak-to-peak pump-voltage swing necessary for a parametric ampli-

[1] A. Uhlir, Jr., "The Potential of Semiconductors in High-Frequency Communications," *Proc. I.R.E.*, Vol. 46, p. 1099, June 1958.

[2] W. Shockley, "The Theory of p-n Junctions in Semiconductors and p-n Junction Transistors," *Bell Sys. Tech. Jour.*, Vol. 28, p. 435, July 1949.

fier to achieve the desired mixing between signal and pump power and to provide gain.

The reverse leakage current through the shunt conductance must be kept low in comparison to the current through the junction capacitance in the operating frequency range. Otherwise, an additional loss is introduced over and above the loss contributed by the total series resistance of the diode, and as a result, the Q of the diode is reduced and the noise figure is increased. The junction capacitance at the bias point is determined by the maximum reverse leakage current allowable for satisfactory circuit performance; in the X-band region, a junction capacitance of 0.5 picofarad or less is required.

Table II—Calculated Values of the Fractional Change of Junction Capacitance of GaAs Diodes for Abrupt and Graded Junctions

ϕ (Volts)	$\triangle C/C$ (Abrupt)	$\triangle C/C$ (Graded)
0.9	0.475	0.350
1.0	0.466	0.342
1.1	0.456	0.334

In small-signal parametric amplifiers, the mixing of the signal and pump frequencies results in maximum power transfer when the phase between the two frequencies is $\pm\pi/2$. Hilibrand and Beam[3] have shown that the total conductance G_t is given by

$$G_t = -\frac{1}{2}\omega_s V_p \frac{dC}{dV} + \frac{\omega_s C}{Q_s} \tag{6}$$

where ω_s is the signal frequency in radians per second, V_p is the pump voltage in volts, and Q_s is the quality factor of the diode at the signal frequency. All quantities are evaluated at the bias point. The first term represents the negative conductance due to the mixing of the two frequencies; the second term is positive and is a measure of the diode loss. For transfer of power from pump to signal frequency, G_t must be negative.

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[3] J. Hilibrand and W. R. Beam, "Semiconductor Diodes in Parametric Subharmonic Oscillators," *RCA Review*, Vol. XX, p. 229, June 1959.

Equation (6) may be used as a guide to optimum design. The total conductance G_t can be made more negative by an increase in either the permissible pump-voltage swing or the capacitance–voltage sensitivity. If the ratio C/Q_s is increased, G_t becomes more positive and the power gain is reduced. For maximum power gain, Q_s should be large and C should be optimized for the circuit employed; there may be no gain if C is too large. For a negative-resistance amplifier, there may be no gain or an actual loss for certain values of V_p, dC/dV, C, and Q_s. Gain may be a rapidly varying function of any of these individual parameters in the region of zero gain.

Design Considerations

As discussed above, total conductance G_t must be negative to achieve gain in a negative-resistance amplifier. Therefore, because the value of C is usually determined by the impedance level required in the circuit, it is desirable to make Q_s, V_p, and dC/dV relatively large.

For high values of Q_s, the capacitance and the diode series resistance must be small. Because electron mobility is greater than hole mobility, an n-type base region is used; its thickness is approximately 3 mils (thinner pellets are more difficult to handle). The thickness of the p-region is usually 0.3 mil or less. The hole mobility is partially compensated by very high surface concentrations (of the order of 10^{20} carriers per cubic centimeter).

The diode series resistance R_d can be separated into two parts, as follows:

$$R_d = R_c + R_m \tag{7}$$

where R_c is the contribution of the contact resistance and R_m is the contribution of the semiconductor material. The following expression for R_m can be obtained from the simple model shown in Figure 4:

$$R_m = \frac{\rho_p x_j}{\pi r_m^2} + \frac{\rho_n x_m}{\pi r_m^2} + \int_0^{x_n} \frac{\rho_n}{A}\, dx. \tag{8}$$

where ρ_p and ρ_n are the resistivities of the p and n regions; r_m is the radius of the mesa in centimeters; x_j, x_m, and x_n are the depths of the junction, the n-doped region, and the base region, respectively; and A is the junction area. The last term in this expression represents the spreading resistance. Because of the impurity-diffusion conditions, ρ_p is usually very small, ρ_n is dictated in part by the breakdown voltage required.

Figure 4 shows several curves of R_m as a function of mesa radius. The mesa area is the dominant factor in the expression for R_m when the resistivities on both sides of the junction are small. Therefore, R_m rises sharply for small mesa radii. When the resistivity on either side of the junction is high, however, R_m is insensitive to mesa radius.

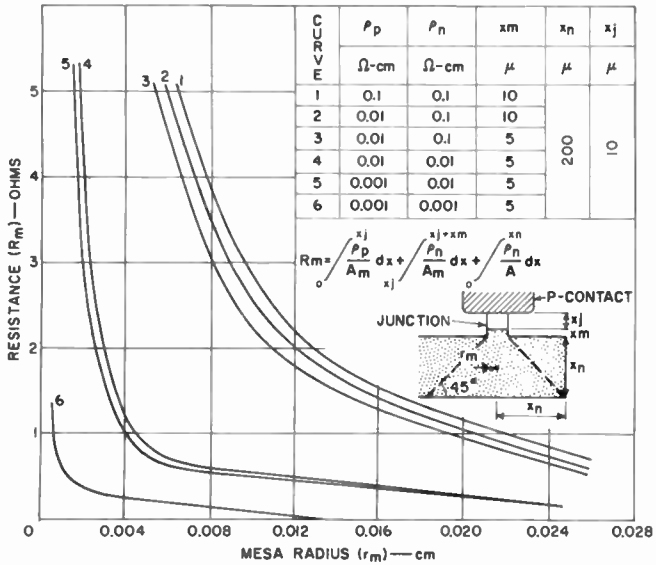

Fig. 4—Resistance of GaAs varactor diode as a function of different parameters.

Contact resistance is usually quite small in germanium and silicon devices, but larger in gallium arsenide units. In the varactor diode shown in Figure 2, R_c is generally of the order of 0.5 ohm when measured under d-c conditions.

For junction penetrations of 0.2 to 0.3 mil, the R_dC product is smallest for values of capacitance less than 1 picofarad. The impedance level in most microwave systems above 1 gigacycle also requires capacitance values less than 1 picofarad. The gallium arsenide varactor diodes described have capacitance values ranging from 0.1 to 1 picofarad. The highest-Q diodes, employing the most up-to-date geometry, usually exhibit values of 0.3 picofarad or less.

The magnitude of the negative conductance G_t is also proportional to the capacitance–voltage sensitivity dC/dV. Equation (6) can be rewritten

$$G_t = -\omega_s C\left(\frac{1}{2}\frac{V_p}{C}\frac{dC}{dV} - \frac{1}{Q_s}\right). \tag{6a}$$

In this equation, the important parameter showing the fractional change of capacitance with respect to voltage is obtained from Equation (4):

$$\frac{1}{C}\frac{dC}{dV} = \frac{n}{\phi_0 - V}. \tag{9}$$

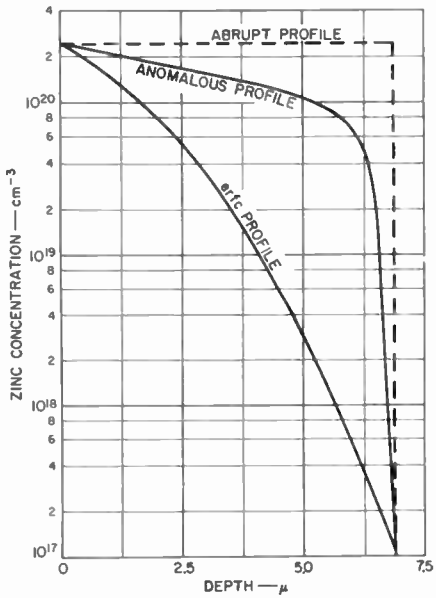

Fig. 5—Typical diffusion profiles for zinc in GaAs.

Figure 5 shows two types of diffusion profiles obtained in gallium arsenide compared with an ideal abrupt junction. The anomalous profile represented by the center curve is obtained by diffusion of zinc into gallium arsenide at temperatures above 850 degrees centigrade.[4] This type of junction approaches the greater capacitance–voltage sensitivity of the abrupt or alloyed junction, but also has the improved uniformity of electrical and metallurgical properties of diffused p-n junctions. Because the diffusion boundary condition is that of an

[4] F. A. Cunnel and G. H. Gooch, "Diffusion of Zinc in Gallium Arsenide," *Jour. Phys. Chem. Solids*, Vol. 15, p. 127, 1960.

infinite source, diffusion would normally result in the error-function complement. The anomalous profile shown in Figure 5 results from the impurity concentration sensitivity of the diffusion coefficient in gallium arsenide at high temperatures.

A compromise must be made in varactor diodes between the series resistance R_d and the breakdown voltage V_B (voltage at which the leakage current is 10 microamperes). The minimum breakdown voltage required to accommodate 200 milliwatts of pump power at 35 gigacycles for an X-band parametric amplifier is approximately 6 volts. This breakdown voltage is achieved by using n-type material with an impurity concentration of approximately 5×10^{17} carriers per cubic centimeter, a junction penetration of 0.2 to 0.3 mil, and a surface concentration of 2×10^{20} carriers per cubic centimeter. Use of a lower impurity concentration in the n-type material, a lower surface concentration, and/or a deeper junction penetration would increase the breakdown voltage, but the series resistance would also increase and the cutoff frequency would be reduced.

Experimental Results

Figure 6 shows the voltage–current characteristics of typical gallium arsenide varactor diodes at four temperatures ranging from 150° to —196°C. These characteristics were measured with only short intervals between temperatures. Applications of thermal shocks in the range between the temperature extremes did not affect the diodes. It can be seen that the variation of breakdown voltage at either temperature extreme is less than 15% of the value at 25°C. Reverse leakage current is less than 10^{-7} ampere for reverse voltages below the breakdown value for temperatures of 100°C or less. The breakdown characteristic is sharp except at temperatures approaching 150°C. The knee of the forward characteristic becomes sharper with decreasing temperature. This effect is caused by an increase in the built-in junction voltage as the temperature is reduced.

Figure 7 shows the junction capacitance as a function of voltage for typical diodes. The solid curves illustrate the range of n-values usually employed for gallium arsenide varactor diodes; the dashed curves represent extreme cases of abrupt and graded junctions. The magnitude of the slope of each curve is proportional to the exponent n; larger slopes result in greater capacitance–voltage sensitivity. It can be seen that the slope of the solid curves is superior to that of graded junctions, and approaches that of abrupt junctions.

The slope of the capacitance curve is also dependent to some extent on the value of ϕ_0, although little effect was noted in Table II in the

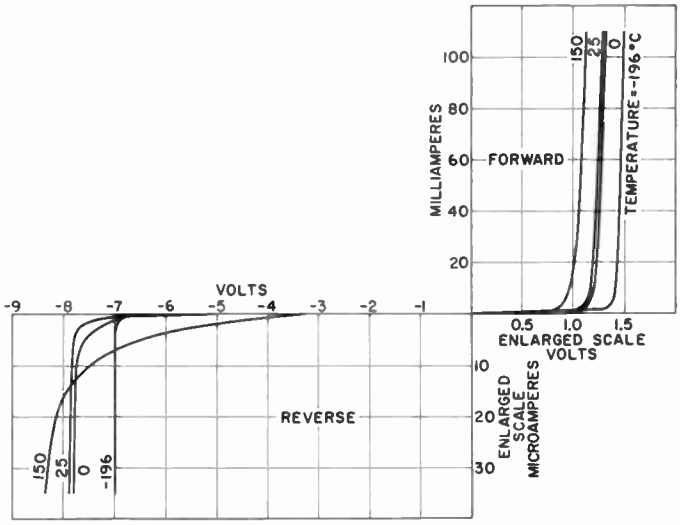

Fig. 6—Typical GaAs varactor diode characteristics at different temperatures.

voltage range from 0.9 to 1.1 volt. Data are usually plotted for several values of ϕ_0, and the value which provides the best straight line is used as the junction built-in potential. This value is usually about 1.0 volt for gallium arsenide devices. The experimental values measured for n indicate that the impurity profile lies between the abrupt and erfc profiles.

In the early stages of the development program, cutoff frequency

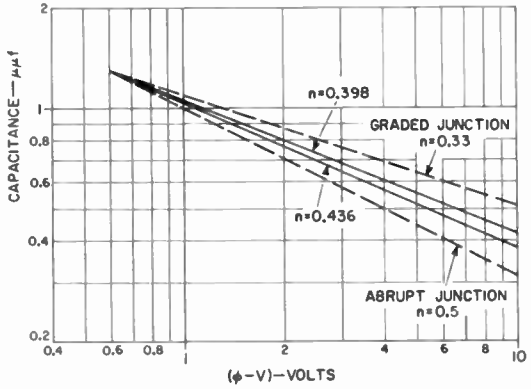

Fig. 7—Junction capacitance as a function of voltage for typical diodes having different n values.

was measured at 2 gigacycles using a slotted line. The equipment used, however, did not give accurate values above 250 gigacycles. Further tests of cutoff frequency were made at 10 gigacycles to obtain accurate values above 250 gigacycles.

The values of cutoff frequency recorded at X-band are derived from the "match technique" described by Houlding.[5] The quality factor Q at a bias of —6 volts is determined from the change ΔQ between —6 volts and the "match bias." On the basis of the capacitance measurements at 1 megacycle, it is possible to calculate the quality factor from the following expression:

$$Q_{-6} = \frac{\Delta Q}{1 - \frac{C_{-6}}{C_0}}. \tag{10}$$

Table III—Measurements of GaAs Varactor Diodes at 10 Gigacycles

Diode No.	V_B (at 10 μa)	C_{-6} (pf)	$\frac{C_{-1} - C_{-6}}{C_{-1}}$	R_s (ohms)	$f_{co(-6)}$ (gigacycles)
#5	10.0	0.30	0.39	3.12	170
#6	10.0	0.24	0.37	3.35	198
#7	11.6	0.35	0.42	2.22	170
#8	11.8	0.24	0.36	1.92	346

Figure 8 shows the normalized impedance as a function of bias for a gallium arsenide varactor diode. It may be seen that the diode series resistance in the reverse direction (where ΔQ is measured) appears to be constant over the range shown (—1 to —7 volts).

Table III shows measurements made on several gallium arsenide varactor diodes at 10 gigacycles and —6 volts. The values of dissipative resistance shown in the table represent total diode and package resistance. Diode #8 represents one of the highest cutoff frequency values measured with the X-band equipment.

Table IV shows typical results obtained when gallium arsenide var-

[5] N. Houlding, "Measurement of Varactor Quality," *Microwave Journal*, Vol. 3, p. 40, Jan. 1960.

Table IV—Performance Data for GaAs Varactor Diodes

Signal Frequency (gigacycles)	9.375	8.7
Pump Frequency (gigacycles)	35.8	35
Gain (db)	15	10
Bandwidth (mc)	16	200
Noise Figure (db)	2.8*	2.9
Pump Power (milliwatts)	125	180

* Includes 0.2 db circulator loss

actor diodes were used in X-band nondegenerative negative-resistance parametric amplifiers. In both cases, the cutoff frequency of the diodes was high enough to permit the use of a pump frequency of 35 gigacycles. In addition, the capacitance–voltage sensitivity of the diodes

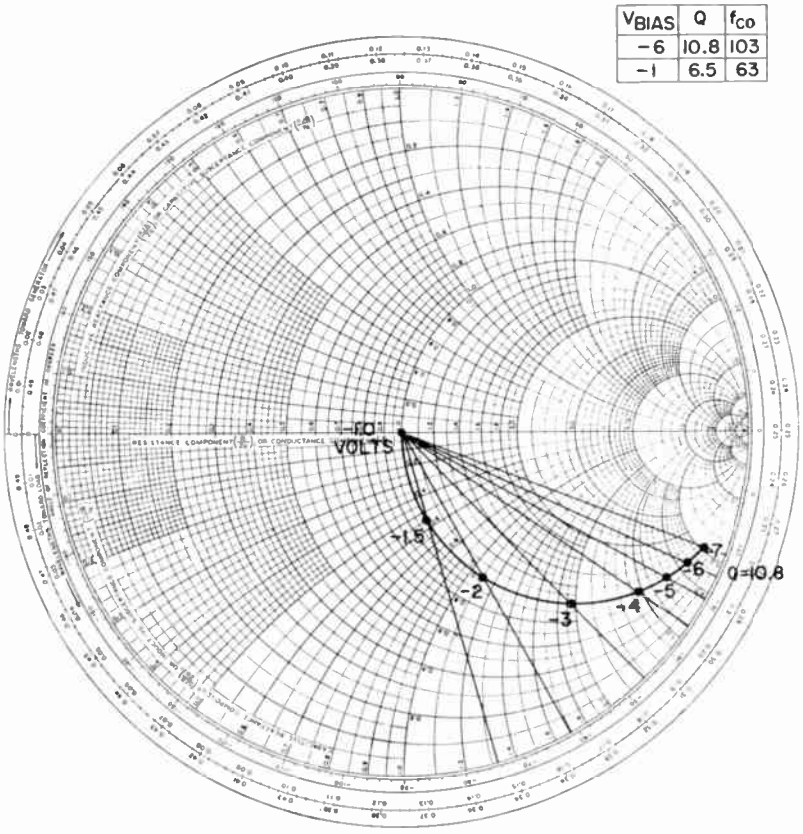

Fig. 8—Normalized impedance curve for GaAs varactor diodes.

permitted the use of a relatively low pump-power level to achieve adequate gain. The capacitance–voltage sensitivity is also reflected to some extent in the low noise figures. If the sensitivity is too low to achieve gain, the pump power must be increased, with an accompanying increase in noise figure.

The noise figure, F, however, is also a function of the factor Q_s, except in cases where the magnitude of the term $(1/C)$ (dC/dV) is low. In such cases, the noise figure will be high and relatively independent of Q_s.

Table V—Performance of GaAs Varactor Diodes in Nondegenerate, Negative-Resistance Amplifier ($f_p = 35.8$ gigacycles, $f_s = 9.375$ gigacycles, Gain = 15 db).

Diode No.	f_{c0}* (gigacycles)	n	Bandwidth (mc)	F (db)	T_n/T_0
#10	266	0.37	9	5.3	2.4
#11	266	0.34	6	6.4	3.4
#12	257	0.32	6	6.4	3.4
#13	238	0.24	5	7.5	4.6
#14	293	0.25	5.5	7.4	4.5
#15	671	0.30	8	6.1	3.1
#16	730	0.34	10	5.1	2.2
#17	150+	0.48	13	3.5	1.2

* Measured at $f = 2$ gigacycles, $V = -1$ volt.

Further tests were made with one of the parametric amplifiers to determine the diode characteristics desirable for low-noise amplification. Table V shows values of normalized noise temperature, T_n/T_0, for several gallium arsenide varactor diodes. There is little correlation between noise temperature and cutoff frequency. However, there is a correlation between noise temperature and the exponent n as shown in Figure 9. These data emphasize the importance of a large capacitance–voltage sensitivity for low-noise amplification. If the pump power has to be increased to achieve gain, the voltage must extend into the forward region to provide greater capacitance–voltage sensitivity. As a result the component of current through the shunt conductance increases, and a source of noise is introduced which would not otherwise be present.

Conclusions

Comparison of the properties of gallium arsenide, germanium, and

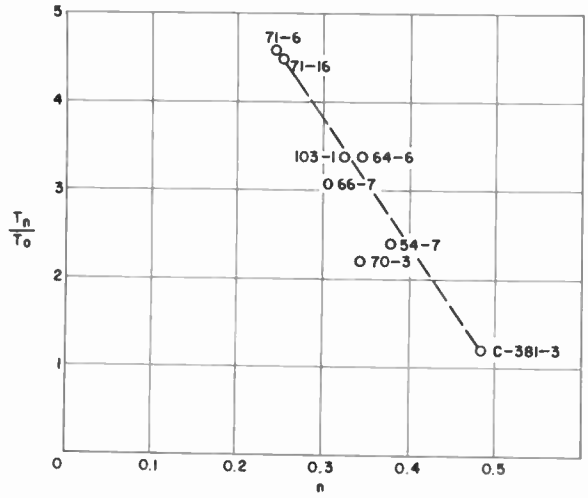

Fig. 9—Correlation between noise temperature and the exponent n.

silicon indicates that gallium arsenide is better suited for devices for which high-frequency, high-power, and/or high-temperature operation are desired. The cutoff-frequency values reported for gallium arsenide are significantly higher than the values reported in the literature for germanium and silicon. In many cases, cutoff frequencies exceed 250 gigacycles. The *V–I* characteristic indicates little change in the temperature range from —196° to approximately 100°C. Cutoff frequency and the capacitance–voltage sensitivity provide adequate figures of merit to guide design considerations for parametric amplifiers utilizing varactor diodes. The resulting circuit performance is outstanding with respect to gain, bandwidth, and noise figure.

ACKNOWLEDGMENT

The authors are pleased to acknowledge the permission of A. Solomon to publish the data in the first column in Table IV and the data in Table V; of R. J. Kampf and V. D. Holaday to publish the data in the second column in Table IV; and of H. C. Lee to publish the data in Table III.

A RIGOROUS ANALYSIS OF HARMONIC GENERATION USING PARAMETRIC DIODES

By

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Summary—A rigorous analysis is given of the operating characteristics of harmonic generators using parametric diodes. The analysis involves a "self-consistent" computation of the interaction between the nonlinear diode and its associated circuits. The computation has revealed many informative aspects which heretofore had remained obscure. Among these is the requirement for a low diode capacitance which is essential to a high-power harmonic generator. In addition, the analysis reveals an optimum circuit condition for maximum power output and efficiency.

Introduction

PARAMETRIC DIODES, which are characterized by nearly lossless reactance, are being widely used as efficient frequency multipliers. The nonlinear interaction of such diodes with circuits for harmonic generation has been analyzed by approximation.[1,2,3] However, this interaction has not been rigorously studied for many recent high-power applications.

The purpose of the present work is to present a rigorous analysis for large-signal harmonic generation using parametic diodes. In essence, the analysis is evolved through a series of "self-consistent" simultaneous computations. First, a set of trial input and output voltages is assumed to drive the parametric diode. The nonlinear charges which appear on the diode are Fourier analyzed. The fundamental and the desired harmonic current components are then obtained. These current components must satisfy the circuit configuration which is defined by the available input power, the bias voltage on the diode,

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[1] K. K. N. Chang, "Harmonic Generation with Nonlinear Reactances," *RCA Review*, Vol. XIX, No. 3, p. 455, Sept. 1958.

[2] J. M. Johnson, "Large Signal Analysis of a Parametric Harmonic Generator," *Trans. I.R.E. Microwave Theory and Techniques*, Vol. MTT-8, p. 525, Sept. 1960.

[3] P. Penfield, Jr., and P. Rafuse, *Varactor Applications*, The MIT Press, Cambridge, Mass., 1962.

and the circuit quality factors (Q's). The reaction of the circuit will result in another set of input and output voltages on the diode which, in general, will not be the same as the original trial ones. Simultaneous computations are cyclically repeated until these two sets of voltages are equal and consistent at an optimum condition of maximum power and efficiency. These voltages are the final correct solutions.

While the large-signal computation presented here is illustrated for the case using a parametric diode, the method can be applied equally well to the general case of any nonlinear-reactance device.

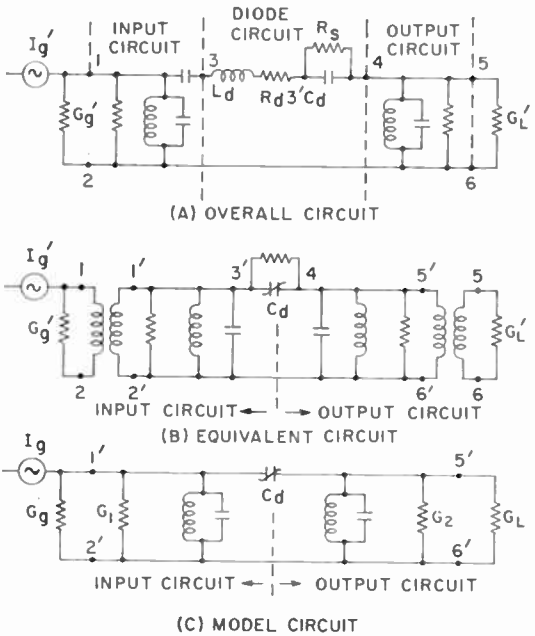

Fig. 1—Equivalent circuit of a harmonic generator using a parametric diode.

Circuit Configuration

Consider an over-all circuit of a harmonic generator using a parametric diode as shown by Figure 1a. The circuit is assumed to support only the fundamental (ω) and the desired harmonic ($n\omega$) components. This mode of operation is achieved by use of adequate filters. The circuit contains an input circuit with a current generator $I_g\cos\omega_1 t$, an output circuit, and a diode circuit. The diode circuit (3-4) is represented by a series lead inductance L_d, a series resistance R_d, a shunt

resistance R_s, and, of course, the diode capacitance C_d, which is responsible for the nonlinear parametric interaction. At resonance, the over-all circuit can be represented by an equivalent circuit (Figure 1b). Note that the diode loss resistances R_d and R_s have been lumped into the total loss resistance by making use of the equivalent circuit. The circuit model to be analyzed is shown by Figure 1c, which is transformed from Figure 1b. G_g and G_L are the generator and load conductances. G_1 and G_2 are the input and output loss conductances, and represent both the circuit and diode losses.

Rigorous Formulation

The parametric diode to be used as the harmonic generator is an abrupt semiconductor p-n junction diode. Such a diode has been shown to be characterized by a voltage-dependent capacitance[4]

$$C_d = \frac{K}{\sqrt{\psi_b - V_e}}, \tag{1}$$

where

$$K = \sqrt{\frac{\epsilon e N_d}{2\left(1 + \frac{N_a}{N_d}\right)}},$$

ϵ is the dielectric constant of the semiconductor material, e is the electronic charge and N_d and N_a are the donor and acceptor concentrations, respectively. V_e is the external bias voltage. ψ_b is the internal built-in junction potential required to set up thermal equilibrium under zero-bias condition. The bias voltage is assumed to be smaller than the breakdown of the diode. In the classical derivation of the quadratic C–V relationship, the external forward bias, V_e, can never exceed the internal potential, ψ_b, for a physical diode exhibiting capacitance. This limitation can be explained as follows: at the p-n junction, due to a high carrier density gradient, electrons diffuse from the n-type material to the p-type material and holes diffuse in the opposite direction. This diffusion process immediately creates a space charge which sets up a strong electric field in a direction such as to oppose the flow of both electrons and holes. An equilibrium is thus maintained, and a depletion-layer capacitance is formed. Now if an external forward electric field

[4] W. Shockley, "The Theory of p-n Junctions in Semiconductors and p-n Junction Transistors." *Bell Syst. Tech. Jour.*, Vol. 28, p. 435, July 1949.

is applied to offset the internal field, the flow of electrons and holes becomes significant, and the capacitance increases to a limiting case when these two fields are equal. Near and beyond the limiting case, the diffusion currents become so large that the capacitance effect no longer exists.

Since the effective electrostatic potential across the junction is $\psi_b - V_e$ when an external bias voltage V_e is applied, the electrostatic charge q_0 on the diode capacitor is

$$q_0 = C_d V = \frac{K}{\sqrt{\psi_b - V_e}} (\psi_b - V_e) = K\sqrt{\psi_b - V_e}. \tag{2}$$

Now suppose that the external bias voltage consists of a d-c voltage V_e, an a-c voltage V_1 at an angular frequency ω_1, and another a-c voltage V_2 at a harmonic frequency $n\omega_1$. Equation (2) then becomes

$$\begin{aligned} q &= K\sqrt{V_0 + V_1 \cos \omega_1 t + V_2 \cos (n\omega_1 t + \theta_1)} \\ &= C_0 V_0 \left[1 + \frac{V_1}{V_0} \cos \omega_1 t + \frac{V_2}{V_0} \cos (n\omega_1 t + \theta_1) \right]^{1/2}, \end{aligned} \tag{3}$$

where $V_0 = \psi_b - V_e$, the total d-c bias, C_0 is the diode capacitance at this d-c bias, and θ_1 is any arbitrary phase angle of the harmonic voltage.

The a-c current I through the diode is

$$\begin{aligned} I = \frac{dq}{dt} = -\frac{\omega_1 C_0 V_0}{2} &\left[\frac{V_1}{V_0} \sin \omega_1 t + \frac{nV_2}{V_0} \sin (n\omega_1 t + \theta_1) \right] \\ &\left[1 + \frac{V_1}{V_0} \cos \omega_1 t + \frac{V_2}{V_0} \cos (n\omega_1 t + \theta_1) \right]^{-1/2}. \end{aligned} \tag{4}$$

Equation (4) represents the sum of all harmonic components resulting from the nonlinear characteristic of the diode. Since the circuitry supports only the fundamental and the desired nth harmonic components, only these two component currents of Equation (4) need be considered.

Self-Consistent Computation

Component currents of the fundamental and the desired harmonic in Equation (4) are nonlinear with respect to their voltages. These currents and voltages must also satisfy the circuit conditions. The

problem cannot be rigorously handled by analytical methods. However, it can be solved by a series of computations. In brief, the computation proceeds as follows: first assume a trial solution, and feed this into the nonlinear equations to be solved and find the solution. Then compare the solution found in this way with the trial one. Many trials may be necessary in order to arrive at a final and self-consistent solution. The computation begins with two sets of current equations, one being the device currents and the other the circuit currents. From Equation (4), the device currents flowing through the diode for the fundamental and the nth harmonic Fourier components are assumed to be, in complex notations,

$$I_1 = j\frac{\omega_1 C_0}{2} V_1 A \exp\{j(\omega_1 t + \phi_1\}, \tag{5}$$

$$I_n = j\frac{n\omega_1 C_0}{2} V_2 B \exp\{j(n\omega_1 t + \phi_2\}, \tag{6}$$

where the voltages V_1A and V_2B and the phase angles ϕ_1 and ϕ_2 are to be determined.

Likewise, at resonance, the circuit currents flowing to the parallel resonant tanks for the fundamental and the nth harmonic are, respectively,

$$I_p = (G_g + G_1)\ V_1 \exp\{j\omega_1 t\}, \tag{7}$$

$$I_q = (G_L + G_2)\ V_2 \exp\{j(n\omega_1 t + \theta_1)\}. \tag{8}$$

The sum of the device resistive currents and circuit resistive currents must satisfy Ohm's law (assuming the circuit is tuned to resonance, making the sum of the reactive currents zero);

$$I_g = (G_g + G_1)\ V_1 - \frac{\omega_1 C_0}{2} V_1 A \sin\phi_1, \tag{9}$$

$$0 = (G_L + G_2)\ V_2 - \frac{n\omega_1 C_0}{2} V_2 B \sin(\phi_2 - \theta_1). \tag{10}$$

For convenience of carrying out the computation, Equations (9) and (10) can be reformulated as

$$\frac{2}{A \sin\phi_1} = X(\theta_1), \tag{11}$$

$$\frac{2}{B \sin (\phi_2 - \theta_1)} = Y(\theta_1), \tag{12}$$

$$\frac{Q_1}{\left(1 - \dfrac{I_g}{V_0(G_g + G_1)} \dfrac{V_0}{V_1}\right)} = M, \tag{13}$$

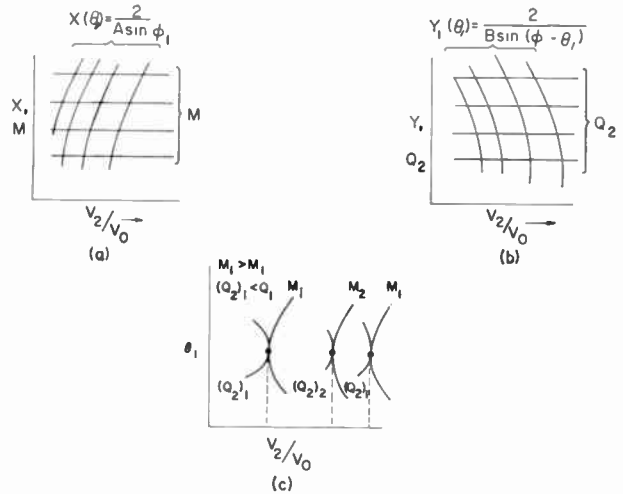

Fig. 2—Self-consistent solutions.

$$\frac{\omega_1 C_0}{G_g + G_1} = Q_1, \tag{14}$$

$$\frac{n\omega_1 C_0}{G_L + G_2} = Q_2, \tag{15}$$

where M is an input current parameter, and Q_1 and Q_2 are circuit quality factors. Equations (11) and (12) enable one to perform a series of self-consistent computations (Figure 2):

(a) By feeding values of V_2/V_0, V_1/V_0, and θ_1 into Equation (4), the fundamental and the nth harmonic current components are found. X and Y as functions of V_2/V_0 and θ_1 are thus determined for various values of M and Q_2.

(b) With a given value of M, a curve of θ_1 versus V_2/V_0 is plotted (Figure 2a).

(c) With a given value of Q_2, a similar curve of θ_1 versus V_2/V_0 is plotted (Figure 2b).

(d) Intersection of constant M and Q_2 curves plotted in steps (b) and (c) determines final solutions of V_1/V_0, V_2/V_0, ϕ_1, ϕ_2, A, and B.

The intersection may take place at more than one point or at no points at all. The optimum solution is the case where these two curves just touch at one point. This point will give the maximum power output and efficiency (Figure 1c). This method combines the principle of self-consistency with simultaneous solutions of the final set of equations.

Power Output and Efficiency

With a given value of V_1/V_0, an optimum curve of Q_2 versus M can be plotted. This Q_2 versus M relationship enables one to compute the power output and efficiency.

The input current can be rewritten as

$$I_g = (G_g + G_1)\left(1 + \frac{G_e}{G_g + G_1}\right)\left(\frac{V_1}{V_0}\right)V_0, \tag{16}$$

where

$$\frac{G_e}{G_g + G_1} = -\frac{Q_1}{2} A \sin\phi_1 = \left[\left(\frac{V_0}{V_1}\right)\frac{I_g}{(G_g + G_1)\,V_0} - 1\right], \tag{17}$$

which gives the ratio of the power transferred to the output harmonic circuit to that dissipated in the generator and the input circuit.

The power output is

$$P_0 = V_2^2 G_L, \tag{18}$$

at an efficiency

$$\eta = \frac{V_2^2(G_L + G_2)}{V_1 I_g}\left(\frac{G_e + G_g + G_1}{G_1 + G_e}\right)\frac{G_L}{G_2 + G_L}$$

$$= \left(\frac{V_2}{V_1}\right)^2 n \frac{B}{A}\frac{\sin(\phi_2 - \theta_1)}{-\sin\phi_1}\left(\frac{G_e}{G_g + G_1}\right)\left(\frac{G_1}{G_1 + G_g} + \frac{G_e}{G_1 + G_g}\right)^{-1}\frac{G_L}{G_2 + G_L}. \tag{19}$$

For the lossless case (i.e., $G_1 = G_2 = 0$), the efficiency must be 100 per cent. Therefore, the factor

$$\left(\frac{V_2}{V_1}\right)^2 n \frac{B}{A} \frac{\sin(\phi_2 - \theta_1)}{-\sin\phi_1}$$

must be unity, or

$$\left(\frac{V_2}{V_1}\right)^2 = \frac{1}{2}\frac{Q_2}{M} \tag{20}$$

from Equations (9), (10), (13) and (15). Equation (19) then reduces to

$$\eta = \frac{G_c}{G_g + G_1}\left(\frac{Q_1}{Q_1'} + \frac{G_e}{G_g + G_1}\right)^{-1}\frac{Q_2}{Q_L}$$

$$= \frac{|A \sin\phi_1|}{|A \sin\phi_1| + \dfrac{2}{Q_1'}}\frac{Q_2'}{Q_L + Q_2'} \tag{21}$$

where

$$Q_1' = \frac{\omega_1 C_0}{G_1},$$

$$Q_2' = \frac{n\omega_1 C_0}{G_2}, \tag{22}$$

$$Q_L = \frac{n\omega_1 C_0}{G_L}.$$

Since both Q_1' and Q_2' are related to the diode series resistance, these two circuit Q's can be written in terms of Q_2 as

$$Q_1' = k_1 Q_2$$

$$Q_2' = k_2 Q_2. \tag{23}$$

k_1 can be either greater or smaller than unity depending on the relative input circuit losses and output circuit losses. k_2 must be greater than unity by definition.

Equations (23) enable one to arrive at two simple normalized expressions for power output and efficiency:

$$\bar{P}_0 = \frac{1}{M} \tag{24}$$

$$\bar{\eta} = \frac{Q_2}{M} \tag{25}$$

where

$$\bar{P}_0 = \frac{P_0}{V_0^2 \omega_1 C_0 \left(\frac{V_1}{V_0}\right)^2 \left(1 - \frac{1}{k_2}\right)} \tag{26}$$

$$\bar{\eta} = \frac{\eta}{\left[\left(1 - \frac{1}{k_2}\right) - \eta\right] k_1}. \tag{27}$$

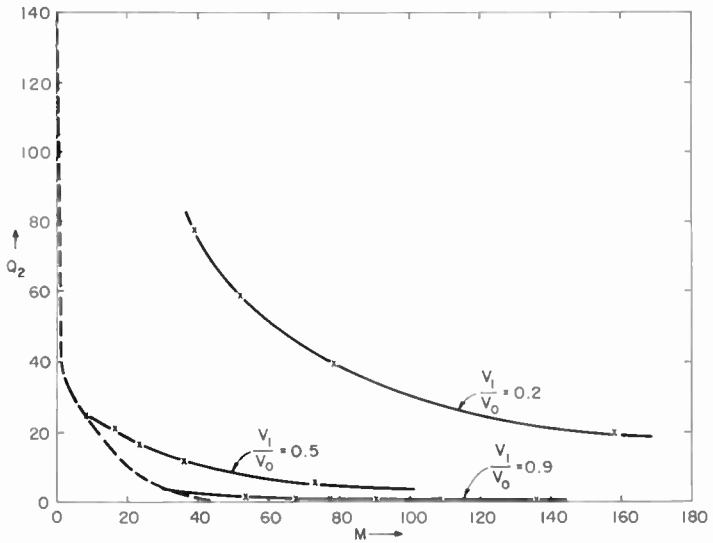

Fig. 3—The output circuit quality factor (Q_2) as a function of the input current parameter (M) at various input voltage drives (V_1/V_0).

RESULTS

For illustration, a doubler was rigorously computed according to the aforementioned method. The Q_2 versus M relationships at various input voltage drives $V_1/V_0 = 0.2$, 0.5 and 0.9 are shown in Figure 3. Power output and efficiency can be calculated and plotted from Equations (24) and (25), as shown in Figure 4.

With a given parametric diode, these characteristic Q_2 versus M curves not only give the optimum relationship between the input source and the output load, but also exhibit a boundary between an allowed region (above the curves) and a stop region (below the curves). On these characteristic curves lie points of maximum power output and

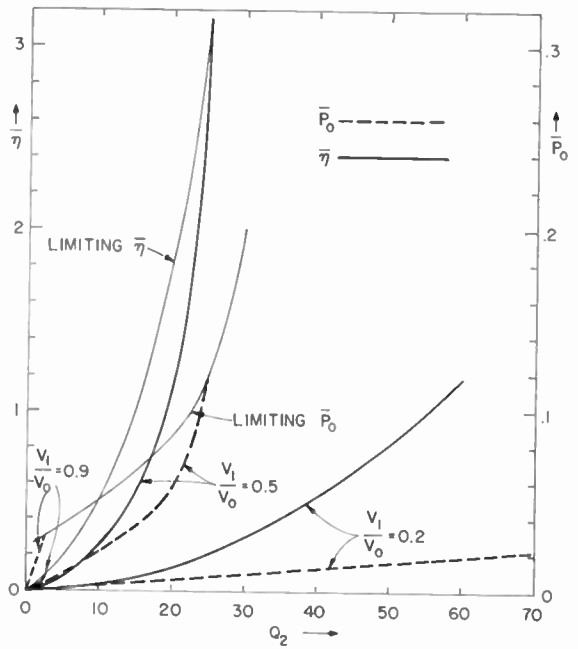

Fig. 4—Normalized power output ($\bar{P}_0$) and efficiency ($\bar{\eta}$) as a function of output circuit quality factor (Q_2).

efficiency. At very low voltage drives, the characteristic curve approximates a hyperbola which can be deduced from the previous small-signal analysis. The curve (dashed line in Figure 3) is another limiting boundary below which the square-root term of Equation (4) becomes imaginary (i.e., the instantaneous value of the voltage drive on the diode exceeds the bias voltage) and the capacitance effect of the diode no longer exists.

The performance characteristic of a parametric diode doubler is shown in Figure 4. As expected, both the normalized power output and efficiency increase as the circuit Q and the input voltage drive. Limiting normalized power output and efficiency occur when the instantaneous voltage drive on the diode equals the bias voltage, as shown by the dashed boundary curves. It is interesting to note that in a low-Q

doubler system, high power output and high efficiency operation is possible only at high input voltage drives (provided the instantaneous voltage drive does not exceed the breakdown of the diode). This is an important guide for harmonic generation at millimeter and submillimeter wave frequencies, at which the circuit Q cannot be expected to be high.

The present theoretical results have been used to compute the characteristics of a previously built 24 to 48 kilomegacycle doubler.[5] The doubler used a gallium arsenide parametric diode which had an internal contact potential (ψ_0) of 1 picofarad. Estimated Q values were $Q_2 = 2$, $Q_2' = 4$, $Q_1' = 8$. The input voltage drive on the diode was of the order of $V_1 = 0.9V_0$. With these circuit parameters, the computed power output and efficiency are, respectively, 1.52 milliwatts and 8.4%. The measured values were 2 milliwatts and 10%.

To generate high-order harmonics, a parametric diode can be operated with a selected output circuit resonant at the particular harmonic of interest. Alternatively, either a series of successive doublers or a multiplicity of harmonic idler resonant circuits may be used. The solution of a series of successive doublers can be readily deduced from the prototype doubler already analyzed. In circuits which employ a multiplicity of harmonic idler resonant circuits, the analytic equations will be the generalizations of Equations (9) and (10):

$$I_g = G_1 V_1 - \frac{\omega_1 C_0}{2} V_1 A \sin \phi_1,$$

$$0 = G_2 V_2 - \frac{2\omega_1 C_0}{2} V_2 B \sin (\phi_2 - \theta_1),$$

$$\vdots$$

$$0 = G_n V_n - \frac{n\omega_1 C_0}{2} V_n N \sin (\phi_n - \theta_{n-1}).$$

The self-consistent computation would be similar to that illustrated in the doubler, although it is more complex. It is reasonable to assume that the efficiency obtained therein should be of the same order of magnitude as that for the case using a sequence of cascaded doublers.

[5] G. H. Heilmeier, "Millimeter Wave Generation by Parametric Methods," *Proc. I.R.E.*, Vol. , p. , July 1960.

Conclusion

The rigorous analysis on harmonic generation with parametric diodes has led to the following informative aspects:

(1) An optimum relationship between the input source and the output load exists for a maximum power output and efficiency.

(2) For high-power and high-efficiency operation in a low-Q system, at millimeter-wave or submillimeter-wave frequencies, high input voltage drives are required.

(3) With parametric diodes of the same cutoff frequency, the power output varies as the cubic power of the junction capacitance. It is thus recommended that diodes of small junction capacitance be used for high power output.

Acknowledgment

The authors wish to thank R. Steinhoff for many helpful discussions.

THE PERFORMANCE OF SUM AND DIFFERENCE MODE PARAMETRIC AMPLIFIERS IN TELEVISION RECEIVERS

By

D. D'Agostini*

Summary—Some salient characteristics of junction-diode parametric amplifiers and their performance at UHF are evaluated in view of their possible use in television receivers. The theory is extended to permit the computation of their performance in the sum, difference, and double-sideband modes. Stable operation is shown to be possible with each mode using different techniques and without the use of expensive isolators or circulators. The noise figure is shown to improve with the use of the difference mode for components of similar quality. However, the pump power required for practical tuners is still considerably beyond the present state of the tunnel-diode art.

Introduction

THE VERY LOW NOISE POSSIBILITIES of parametric amplifiers, which can be obtained without resorting to very low temperatures or high focusing fields, promise a major improvement in communication systems. Extensive work has been done in this field and no outstanding difficulty can be foreseen in applying parametric devices to television receivers. A careful analysis of the requirements imposed on devices for television receivers indicates, however, that most of these requirements have not been previously considered and are not fulfilled by devices which have been reported. In this paper some salient characteristics of junction-diode parametric amplifiers are analyzed and their potential performance evaluated within the framework of their application to television receivers.

Due to their low losses, semiconductor junctions with nonlinear capacitance are considered most desirable for parametric amplifiers using nonlinear reactances. Nonlinear inductances (ferrites) appear to be too lossy for low-noise applications at UHF frequencies.

Theory

The following periodic signal components are present across the junction diode:

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ω_s : fundamental signal frequency,

ω_p : fundamental pump frequency,

$\pm \omega_s \pm \omega_p$: pump and signal sums and differences,

$\pm \omega_s \pm n\omega_p$: pump harmonics and signal sums and differences.

The signal harmonics are disregarded because the signal amplitude is assumed to be very small compared with that of the pump frequency. Under these conditions, the incremental voltage across the diode is

$$dv = \sum_{n=-\infty}^{\infty} \sum_{m=-1}^{1} V_{n,m} \exp\{j(nx + my)\}, \tag{1}$$

where

$$x = \omega_p t,$$

$$y = \omega_s t,$$

$$V_{n,m} = V^*_{-n,-m}, \tag{2}$$

since dv is real. The incremental diode charge is similarly periodic and can be written

$$dq = \sum_{n=-\infty}^{\infty} \sum_{m=-1}^{1} Q_{n,m} \exp\{j(nx + my)\}, \tag{3}$$

where

$$Q_{n,m} = Q^*_{-n,-m},$$

since dq is real. The incremental voltage and charge are related by

$$dq = C(v,t)\,dv. \tag{4}$$

The diode capacitance is periodic at the pump frequency;

$$C(v,t) = \sum_{n=-\infty}^{\infty} C_n \exp\{jnx\} \tag{5}$$

where

$$C_n = C^*_{-n} = \frac{1}{2\pi} \int_0^{2\pi} C(v,t) \exp\{-jnx\}dx. \tag{6}$$

From Equations (1), (3), and (4),

$$\sum_{n=-\infty}^{\infty} \sum_{m=-1}^{1} Q_{n,m} \exp\{j(nx+my)\} = \sum_{p=-\infty}^{\infty} C_p \exp\{jpx\}$$

$$\sum_{r=-\infty}^{\infty} \sum_{m=-1}^{1} V_{r,m} \exp\{j(rx+my)\}. \qquad (7)$$

The diode current is given by the derivative of Equation (7);

$$\sum_{n=-\infty}^{\infty} \sum_{m=-1}^{1} I_{m,n} \exp\{j(nx+my)\} =$$

$$\sum_{r=-\infty}^{\infty} \sum_{p=-\infty}^{\infty} \sum_{m=-1}^{1} j[(r+p)\omega_p + m\omega_s] C_p V_{r,m} \exp\{j[(r+p)x+my]\}. \qquad (8)$$

Therefore the current components are given by

$$In\omega_p + \omega_s = \sum_{p=-\infty}^{\infty} j(n\omega_p + \omega_s) C_p V_{(n-p)\omega_p+\omega_s}, \qquad (9)$$

with a similar expression for $m = -1$. The corresponding matrix is given in Equation (10).

This infinite matrix gives the relations among the infinite number of components generated by pumping. It has been recognized that among all the possible signal combinations, two particular combinations (modes) are of special interest.[1-3a] They will be first considered separately and then in combination. Signal with other frequencies will be neglected because the actual circuit prohibits their existence or at least substantially attenuates their effect.

Sum-Mode Parametric Amplifier

Theory

A schematic of a parametric amplifier pertinent to both sum and difference mode operation is shown in Figure 1. Three signal com-

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[1] J. M. Manley and H. E. Rowe, "Some General Properties of Nonlinear Elements—Part I, General Energy Relations," *Proc. I.R.E.*, Vol. 44, p. 904, July 1956.

[2] S. Bloom and K. K. N. Chang, "Theory of Parametric Amplification Using Nonlinear Reactances," *RCA Review*, Vol. 18, p. 578, Dec. 1957.

[3] H. E. Rowe, "Some General Properties of Nonlinear Elements—Part II, Small Signal Theory," *Proc. I.R.E.*, Vol. 46, p. 850, May 1958.

[3a] L. A. Harwood and T. Murakami, "An Experimental Parametric Tuner for UHF Television Receivers," *RCA Review*, Vol. XXIV, p. 253, June 1963.

$$
\begin{vmatrix} \cdot \\ \cdot \\ \cdot \\ I_{2\omega_p+\omega_s} \\ I_{\omega_p+\omega_s} \\ I_{\omega_s} \\ I^*_{\omega_p-\omega_s} \\ I_{2\omega_p-\omega_s} \\ \cdot \\ \cdot \\ \cdot \end{vmatrix} = \begin{vmatrix} \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot \\ \dots j(2\omega_p+\omega_s)C_0 & j(2\omega_p+\omega_s)C_1 & j(2\omega_p+\omega_s)C_2 & j(2\omega_p+\omega_s)C_3\dots \\ \dots j(\omega_p+\omega_s)C^*_1 & j(\omega_p+\omega_s)C_0 & j(\omega_p+\omega_s)C_1 & j(\omega_p+\omega_s)C_2\dots \\ \dots j(\omega_s)C^*_2 & j(\omega_s)C^*_1 & j(\omega_s)C_0 & j(\omega_s)C_1\dots \\ \dots j(\omega_p-\omega_s)C^*_3 & j(\omega_p-\omega_s)C^*_2 & j(\omega_p-\omega_s)C^*_1 & j(\omega_p-\omega_s)C_0\dots \\ \dots j(2\omega_p-\omega_s)C^*_4 & j(2\omega_p-\omega_s)C^*_3 & j(2\omega_p-\omega_s)C^*_2 & j(2\omega_p-\omega_s)C^*_1 \\ \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot \end{vmatrix} \begin{vmatrix} \cdot \\ \cdot \\ \cdot \\ V_{2\omega_p+\omega_s} \\ V_{\omega_p+\omega_s} \\ V_{\omega_s} \\ V^*_{\omega_p-\omega_s} \\ V^*_{2\omega_p-\omega_s} \\ \cdot \\ \cdot \\ \cdot \end{vmatrix}
$$

(10)

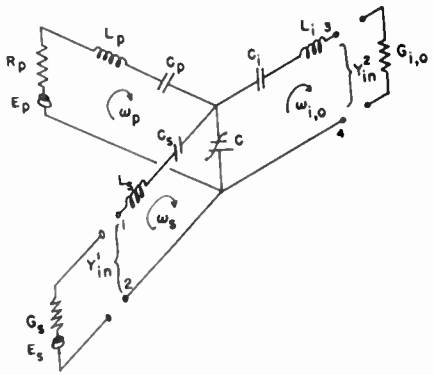

Fig. 1—Parametric amplifier schematic.

ponents flow in the common nonlinear capacitance: the pump frequency is ω_p, the input signal ω_s, and the output signal $\omega_0 = \omega_p + \omega_s$.

The general matrix reduces to a 2 × 2 matrix;

$$\begin{vmatrix} I_{\omega_0} \\ I_{\omega_s} \end{vmatrix} = \begin{vmatrix} j\omega_0 C_0 & -j\omega_0 \lambda V_{\omega_p} \\ -j\omega_s \lambda V_{\omega_p} & j\omega_s C_0 \end{vmatrix} \begin{vmatrix} V_{\omega_0} \\ V_{\omega_s} \end{vmatrix} \tag{11}$$

where the diode capacitance is taken as

$$C(v,t) = C_0 - \lambda V_{\omega_p} \exp\{j\omega_p t\}, \tag{12}$$

hence

$$C_1 = -\lambda V_{\omega_p}. \tag{13}$$

Junction diode losses are represented in Figure 2. The effect of the losses may be lumped in a parallel conductance. A lossless network is

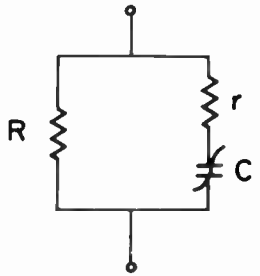

Fig. 2—Lossy junction diode.

shown in Figure 3, and a network where the diode losses are lumped in G_1^D and G_2^D is shown in Figure 4. The circuit losses are lumped in G_1 and G_2.

The network admittance matrix can be written

$$Y = \begin{vmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{vmatrix}. \tag{14}$$

The input admittance seen between points 1 and 2 in Figure 4 is

$$Y_{in} = Y_{11} - \frac{Y_{12}\,Y_{21}}{Y_{22} + G_0}. \tag{15}$$

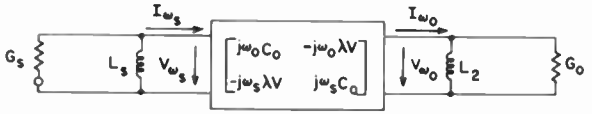

Fig. 3—Lossless parametric amplifier.

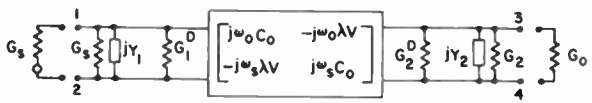

Fig. 4—Parametric amplifier with losses.

The input admittance seen between points 3 and 4 is

$$Y_{out} = Y_{22} - \frac{Y_{12}\,Y_{21}}{Y_{11} + G_s}. \tag{16}$$

The power gain is

$$G = \frac{4\,|Y_{21}|^2\,G_0 G_s}{|\,(G_0 + Y_{21})\,(G_s + Y_{in})\,|^2}. \tag{17}$$

The admittance matrix of the amplifier shown in Figure 4 is

$$Y = \begin{vmatrix} j\omega_s C_0 + G_1^D + G_1 + jY_1 & -j\omega_s\lambda V \\ -j\omega_0\lambda V & j\omega_0 C_0 + G_2^D + G_2 + jY_2 \end{vmatrix} \tag{18}$$

When the input and output are tuned,

$$jY_1 = -j\omega_s C_0,$$
$$jY_2 = -j\omega_0 C_0.$$

Then

$$Y_{11} = G_1{}^D + G_1 = y_{11},$$
$$Y_{12} = -j\omega_s \lambda V = -jy_{12},$$
$$Y_{21} = -j\omega_0 \lambda V = -jy_{21}, \tag{19}$$
$$Y_{22} = G_2{}^D + G_2 = y_{22},$$

and

$$Y_{in} = y_{11} + \frac{y_{12}\, y_{21}}{G_0 + y_{22}}, \tag{20}$$

$$Y_{out} = y_{22} + \frac{y_{12}\, y_{21}}{G_s + y_{11}}. \tag{21}$$

The gain is

$$G = \frac{4G_0 G_s \, |y_{21}|^2}{[(G_s + y_{11})(G_0 + y_{22}) + y_{12}y_{21}]^2}. \tag{22}$$

An optimum gain is obtained for an optimum source conductance;

$$G'_s = \left[y_{11}{}^2 + \frac{y_{11}}{y_{22}} y_{12}y_{21} \right]^{1/2}, \tag{23}$$

and an optimum load conductance

$$G'_0 = \left[y_{22}{}^2 + \frac{y_{22}}{y_{11}} y_{12}y_{21} \right]^{1/2}. \tag{24}$$

The following quality factors are introduced: q_1 for the input circuit, q_2 for the output circuit, and Q_1 for the diode, at the input frequency (ω_s); and the following parameters are defined:

$$k = \frac{\omega_2}{\omega_1}, \tag{25}$$

$$\tau_1 = \frac{1}{q_1} + \frac{1}{Q_1} = \frac{G_1 + G_1{}^D}{\omega_s C_0}, \tag{26}$$

$$\tau_2 = \frac{k}{q_2} + \frac{k^2}{Q_1} = \frac{G_2 + G_2{}^D}{\omega_s C_0}, \tag{27}$$

$$K^2 = \omega_s \omega_0 \omega \overline{V}^2. \tag{28}$$

The optimum load and source conductance become

$$G'_s = \left[(C_0 \omega_s)^2 \tau_1 + \frac{\tau_1}{\tau_2} K^2 \right]^{1/2}, \tag{29}$$

$$G'_0 = \left[(C_0 \omega_s)^2 \tau_2 + \frac{\tau_2}{\tau_1} K^2 \right]^{1/2}. \tag{30}$$

For good diodes

$$(C_0 \omega_s)^2 \tau_1 \ll \frac{\tau_1}{\tau_2} K^2, \tag{31}$$

$$(C_0 \omega_s)^2 \tau_2 \ll \frac{\tau_2}{\tau_1} K^2. \tag{32}$$

Then Equations (29) and (30) become

$$G'_s \cong \sqrt{K \frac{\tau_1}{\tau_2}}, \tag{33}$$

$$G'_0 \cong \sqrt{K \frac{\tau_2}{\tau_1}}. \tag{34}$$

If

$$p = \frac{C_0 \omega_s}{K} \sqrt{\tau_1 \tau_2}, \tag{35}$$

the optimum gain becomes

$$\text{gain} = \frac{k}{\left(\frac{1}{2} p^2 + p + 1 \right)^2}. \tag{36}$$

For small losses,

$$\text{gain} = k(1 - 2p). \tag{37}$$

Note that the product of G_s and G_0 equals K^2—the result for optimum gain and bandwidth derived by Rowe for the lossless case,[3] although here $K \neq G_s \neq G_0$. The gain becomes $k = \omega_0/\omega_s$ in the lossless case, as required by the Manley–Rowe equation.[1]

Noise Factor

The noise factor is given by

$$\begin{aligned} F &= 1 + \frac{G_1 + G_1{}^D}{G_s} + \frac{1}{k}\,\frac{G_2 + G_2{}^D}{K^2}\,\frac{(G_s + G_1 + G_1{}^D)}{G_s}^2 \\ &= 1 + \frac{\omega_s C_0}{G_s}\left[\tau_1 + \frac{\tau_2}{k}\,\frac{G_s + \tau_1 + \omega_s C_0}{K}\right]^2. \end{aligned} \tag{38}$$

The noise factor is minimum for an optimum value of the source conductance,

$$G_s{}^1 = \left[(\tau_1 C_0 \omega_s)^2 + kK^2\,\frac{\tau_1}{\tau_2}\right]^{1/2}. \tag{39}$$

The over-all system noise factor is given as usual by

$$F_{ov} = F_1 + \frac{F_{i\text{-}f} - 1}{G}, \tag{40}$$

where G is the parametric stage gain and $F_{i\text{-}f}$ is the noise figure of the following stage.

A sum-mode parametric amplifier may be designed for use with television receivers. Figure 5 shows an "autonomous" version and Figure 6 shows an "imbedded" version. Autonomous preamplifiers can tolerate a moderate pump-frequency shift and require a unique pump source. Imbedded preamplifiers require two different pump sources whose frequencies are such that the output frequency is 45 mc (the television-receiver i-f), for any input signal frequency. In this case the frequency of the pumps becomes critical; a supplementary UHF oscillator can be added to monitor the two pumps and improve the frequency stability.

In both versions the output frequency of the parametric amplifier is in the microwave range and is converted down by a crystal-diode mixer. In the autonomous version, this mixer is followed by a television-receiver front end. The best noise figure of UHF television receivers is 9 db, and the corresponding best crystal-diode mixer noise

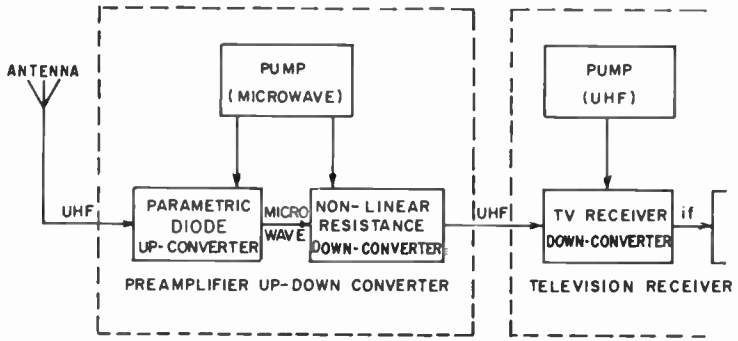

Fig. 5—Autonomous preamplifier.

figure is plotted versus frequency in Figure 7. In the imbedded version, the mixer is followed by a receiver i-f stage. The best noise figure of the i-f stage is about 3 db, and the corresponding best crystal-diode mixer noise figure is also plotted versus frequency in Figure 7.

The parametric amplifier has higher gain when the output frequency is higher, but then the noise figure of the crystal-diode mixer deteriorates, as seen in Figure 7. The values of 5, 10, and 20 kilomegacycles appear to cover a practical range of output frequency.

For lossless parametric diodes, the gain is equal to the ratio of output to input frequency and, since the diode is noiseless, the noise figure is simply unity (0 db). In this case a simple computation can be used to determine the optimum over-all noise figure. This over-all system noise figure is plotted in Figure 8. This theoretical value is not attainable in practice, when diodes and circuit losses are present.

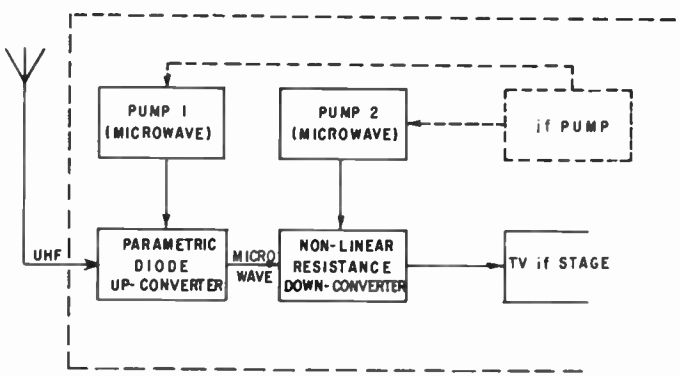

Fig. 6—Imbedded preamplifier.

It is recalled here that a pure sum-mode operation has been assumed, and that the presence of spurious modes can also alter these results.

In order to evaluate the over-all noise figure when losses are included, three parameters have been varied: R, the diode parallel resistance; r, the diode series resistance; λV, equal to half the peak to peak diode capacitance change due to the pump voltage swing (V).

A typical diode with $C_0 = 1$ picofarad has been chosen, and the

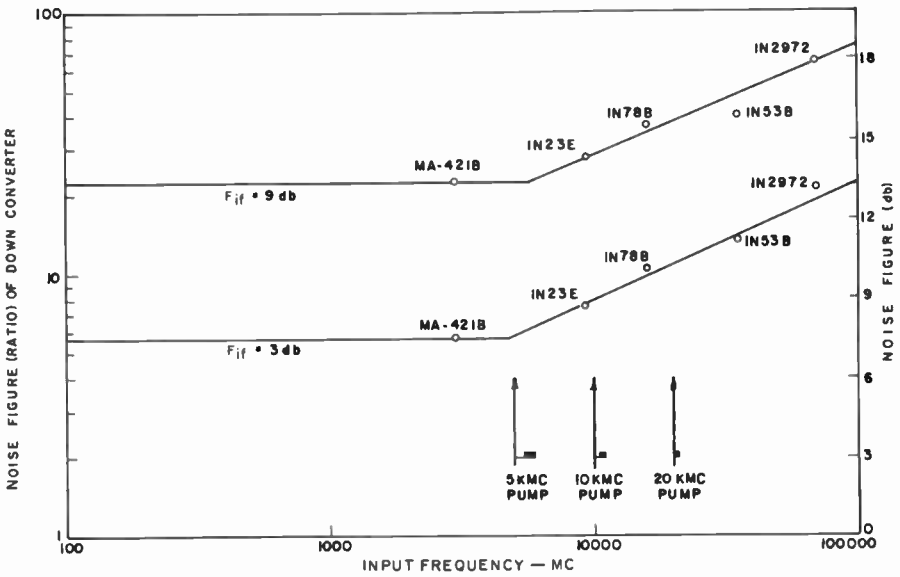

Fig. 7—Noise figures of best available microwave mixers for i-f noise figures of 3 db and 9 db.

above parameters yield effective upper frequency cutoffs of 37.5, 75, and 150 kmc, and effective lower frequency cutoffs of 3.2, 6.4, and 12.8 mc. By proper choice of R and r, the circuit losses may be included. The effective capacitance nonlinearity (λV) is varied from the poorest to the best practical values.

The noise figure for the matched case is plotted versus frequency in Figure 9 for both the autonomous and imbedded versions, and the noise figure for the optimum mismatch is plotted in Figure 10. The curves were obtained for $\lambda V = 0.2$ picofarad, $C_0 = 1$ picofarad, $r = 2.12$ ohms and $R = 25000$ ohms.

For a constant input frequency of 1 kmc and an up-converter output frequency of 10 kmc, the noise figure is plotted versus relative

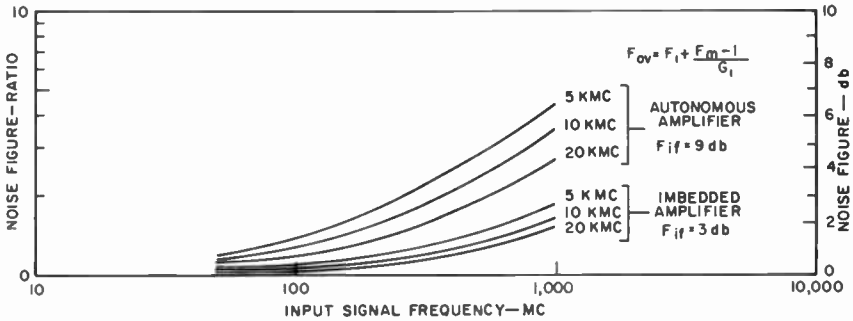

Fig. 8—Over-all noise figure for lossless parametric sum-mode up-converter.

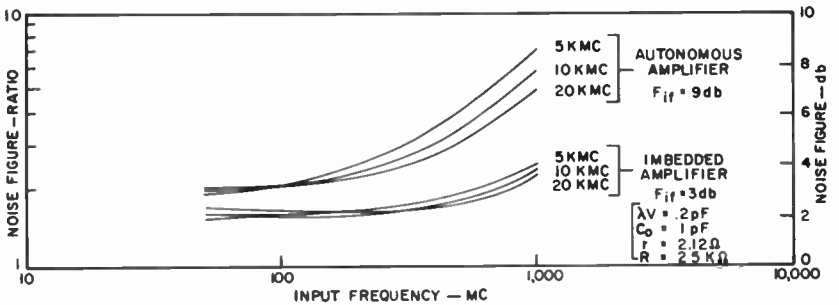

Fig. 9—Over-all noise figure for matched input parametric sum-mode up-converter.

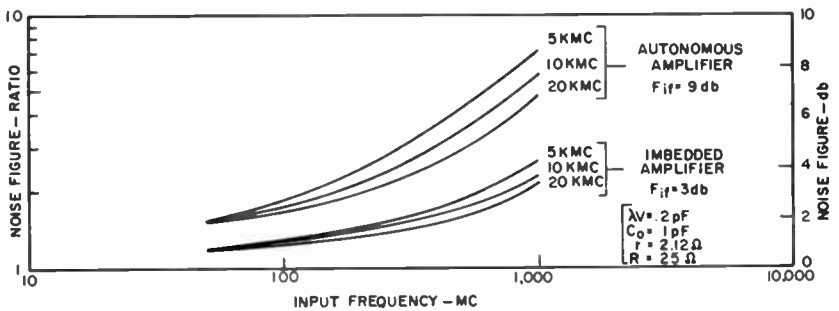

Fig. 10—Optimum-mismatch over-all noise figure for parametric sum-mode up-converter with loss.

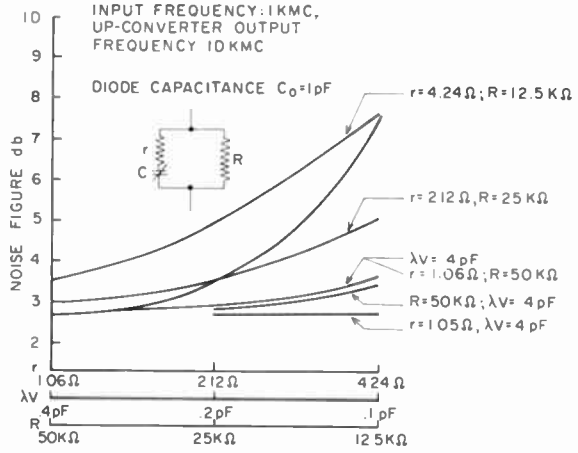

Fig. 11—Imbedded preamplifier over-all noise figure ($F_{i-f} = 3$ db).

values of the three parameters in Figure 11 for the imbedded version, and in Figure 12 for the autonomous version.

The autonomous and imbedded preamplifier curves are neatly separated into two groups in all cases. The price paid in higher values of noise figure for the stage following the crystal diode mixer is apparent. This is mainly due to the limited gain of the up-converter.

Experiments

An experimental separate VHF preamplifier, shown in Figure 13,

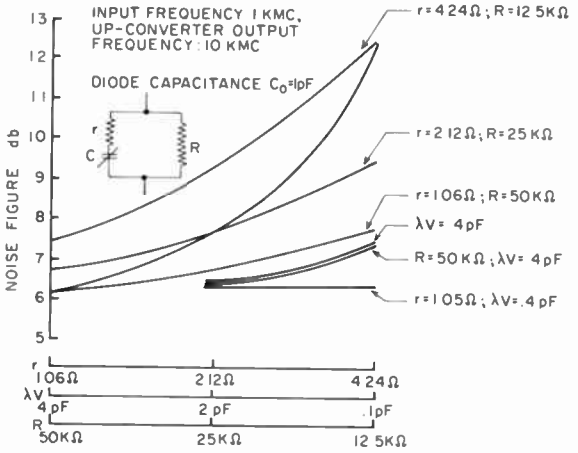

Fig. 12—Autonomous preamplifier over-all noise figure ($F_{i-f} = 3$ db).

was built and the following performance was obtained:

Input (1) signal frequency	:	83 mc
Output(1) signal frequency	:	803 mc
Pump frequency (P)	:	720 mc
Input(2) signal frequency	:	803 mc
Output(2) signal frequency	:	83 mc
Bandwidth (3 db down)	:	12.7 mc
Input(1) to output(2) gain	:	5.2 db
Output(2) to input(1) loss	:	14.8 db
Noise figure of receiver	:	$F_{i\text{-}f} = 4.2$ db
Noise figure at input(2)	:	$F_m = 10.1$ db
Noise figure at input (1)	:	$F_{ov} = 3$ db
Input(2) to output(2) conversion loss	:	6 db
Input(1) to output(1) gain	:	11.2 db
Parametric diodes	:	$f_c = 64$ and 81 kmc
Crystal mixers	:	1N21B

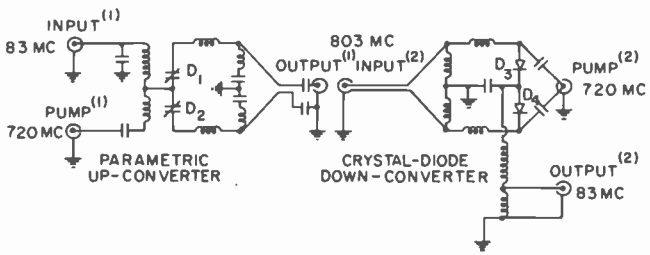

Fig. 13—Separate parametric up-converter.

The preamplifier was found to be unconditionally stable and matched, and to have sufficient signal-power capability. When the pump frequency and the i-f noise factor are taken into account, the measured noise figure is seen to fit satisfactorily the computed curves of Figure 9. Investigations of the sum mode have shown the following advantages:

1. Low noise figure,
2. Unconditionally stable (positive-resistance operation),
3. Input and output match possible,
4. Stable gain (relative to pump signal drive),
5. Good forward-to-backward gain ratio,

6. Broad bandpass,
7. Good signal-power capability;

and the following disadvantages:

1. Elimination of the difference mode is elaborate with large-bandwidth circuits,
2. Spurious mode(s) may result from mere diode bias and/or pump drive with reduced stability,
3. Gain is limited to output-to-input signal frequency ratio,
4. Spurious resonances at the output signal frequency occur in the input circuit. Pump circuit couplings at input and output are troublesome,
5. Very-high-quality diodes are required,
6. The output signal frequency is much higher than the input signal frequency.

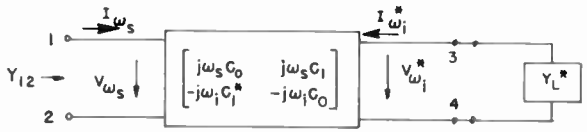

Fig. 14—Two-terminal-pair linear network.

Difference Mode Parametric Amplifier

Theory

The three signal components flowing in the common linear capacitance of the parametric amplifier shown in Figure 1 are now the pump (ω_p), the input signal (ω_s), and the idler ($\omega_i = \omega_p - \omega_s$).

The general matrix reduces now to:

$$\begin{vmatrix} I_{\omega_s} \\ I^*_{\omega_i} \end{vmatrix} = \begin{vmatrix} j\omega_s C_0 & -j\omega_s \lambda V \\ +j\omega_i \lambda V & -j\omega_i C_0 \end{vmatrix} \begin{vmatrix} V_{\omega_s} \\ V^*_{\omega_i} \end{vmatrix} \tag{41}$$

The parametric stage is shown in Figure 14 as a two-terminal pair network. The diode series resistance, r, and the idler series resistance, R, are regarded as part of the idler, as shown in Figure 15. The network has also been modified to extract C_0 and r from the 1′,2′ and 3′,4′ network as shown.

The new network input admittance is obtained:

$$Y_{1'2'} = -\frac{\omega_s \omega_i |\lambda V|^2}{Y'^{*}_{L}}. \tag{42}$$

Near resonance of Y'_L, $Y_{1'2'}$ becomes real and has the value

$$Y_{1'2'} = -2\pi f_{c0} \frac{\omega_s}{\omega_i} \frac{(\lambda V)^2}{C_0}. \tag{43}$$

The noise generated by this negative conductance is due to the idler-resistances, and is therefore reduced by the frequency ratio ω_i/ω_s

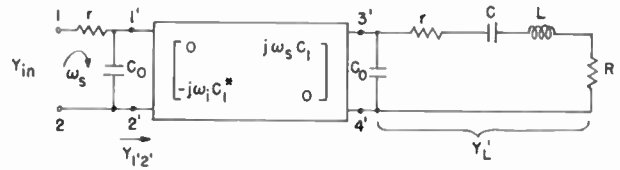

Fig. 15—Parametric difference-mode with losses.

according to the Manley and Rowe equations.[1] Hence its equivalent noise temperature is

$$T = T_0 \frac{\omega_i}{\omega_s}. \tag{44}$$

The noise temperature found across 1,2 is increased by the contribution of the diode series resistance r which remains at room temperature.

Hybrid Junctions

Simple negative-resistance amplifiers are inherently unstable; suitable stabilizing techniques are therefore necessary. This problem is usually solved by using circulators, isolators, impedance inverters, or hybrid junctions. The hybrid junctions offer a promising solution, because they can be inexpensive and also allow for variation of the amplifier gain without loss of stability.[4-7]

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[4] R. W. P. King, *Transmission Line Theory*, McGraw Hill, p. 199, 1955.

[5] H. G. Pascalar, "Strip Line Hybrid Junctions," *I.R.E. Trans. PGMTT*, Vol. MTT-5, p. 23, Jan. 1957.

[6] T. Morita and L. S. Seingold, "A Coaxial Magic-T," *I.R.E. Trans. PGMTT*, Vol. MTT-1, p. 17, Nov. 1953.

[7] D. Sahib, "Broadband Hybrid-Coupled Parametric Amplifier," *Microwave Jour.*, Vol. 5, p. 87, May 1962.

A difference-mode parametric amplifier using a hybrid junction is shown in Figures 16 and 17. A symbolic diagram of a hybrid junction is shown in Figure 18, with appropriate parameters. Figure 19 shows a two $\lambda_0/4$ hybrid-junction version which can be realized inexpensively with a double concentric coaxial line.[7]

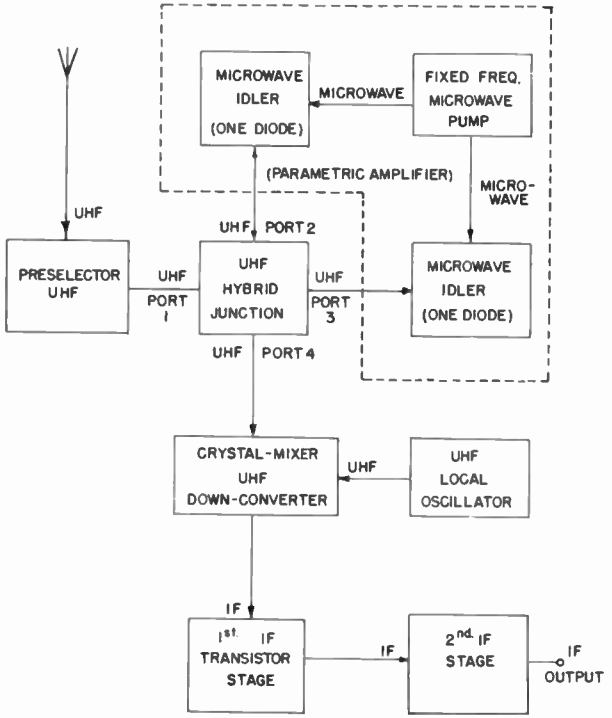

Fig. 16—UHF parametric-amplifier block diagram.

The two $\lambda_0/4$ hybrid junctions can be represented by the matrix

$$\begin{vmatrix} V_{r_1} \\ V_{r_2} \\ V_{r_3} \\ V_{r_4} \end{vmatrix} = \begin{vmatrix} 0 & -j(1/2) & 1/2 & 0 \\ -j & 0 & 0 & 1/2 \\ 1 & 0 & 0 & -j(1/2) \\ 0 & 1 & -j & 0 \end{vmatrix} \begin{vmatrix} V_{i_1} \\ V_{i_2} \\ V_{i_3} \\ V_{i_4} \end{vmatrix} \tag{45}$$

With the reflection coefficient ρ_j at ports 2,3, and 4,

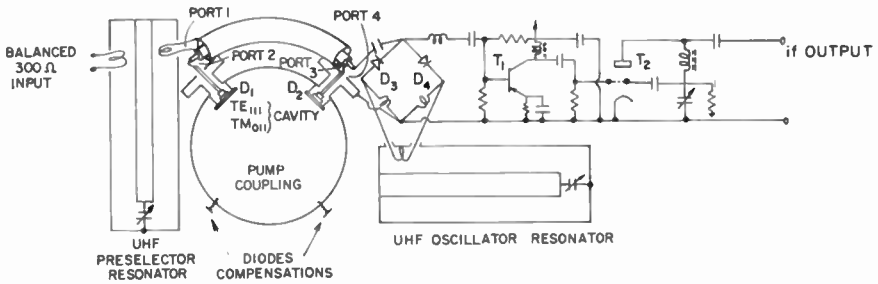

Fig. 17—Parametric amplifier for UHF television.

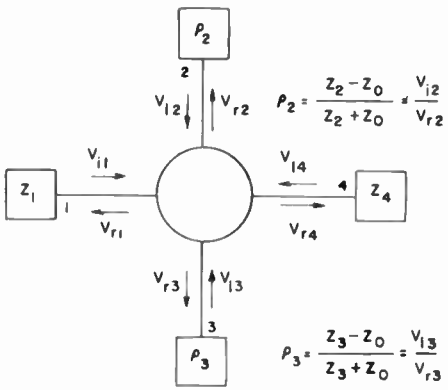

Fig. 18—Symbolic diagram of a hybrid junction.

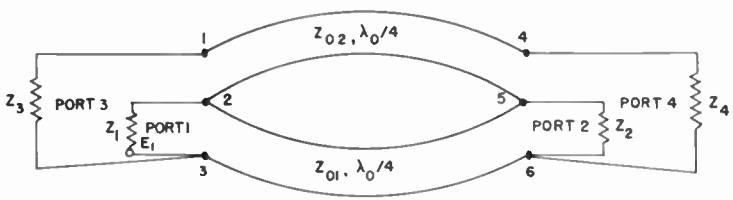

Fig. 19—Two $\lambda_0/4$ hybrid junction.

$$\rho_j = \frac{Z_j - Z_0}{Z_j + Z_0}, \quad j = 2,3,4, \tag{46}$$

the power gain is

$$G = \frac{\left(\frac{\rho^3 - \rho^2}{2}\right)^2}{\left[1 + \rho_4 \frac{\rho_3 - \rho_2}{2}\right]^2}, \tag{47}$$

which reduces to:

$$G = |\rho|^2 \tag{48}$$

for $\rho_2 = \rho_3 = \rho$.

When ports 2 and 3 are terminated by negative conductances, the gain of the amplifier is greater than unity because $|\rho| > 1$.

The input reflection coefficient is

$$\rho_{in} = \frac{V_{r_1}}{V_{i_1}} = \frac{\rho_3 - \rho_2}{2} - \rho_4 \frac{\left(\frac{\rho^3 - \rho^2}{2}\right)^2}{\left(\rho_4 \frac{\rho_3 - \rho_2}{2} + 1\right)^2}. \tag{49}$$

Analysis of Equation (49) shows that the amplifier can be matched when the two negative conductances are equal ($\rho_2 = \rho_3$) and the output stage presents a match ($\rho_4 = 0$). The amplifier remains stable and immune to the source-impedance variation as long as the input reflection coefficient is smaller than unity.

Noise Figure

The noise figure of the parametric-amplifier stage is influenced by the reflection coefficient at each port and the noise temperature of the termination at that port,

$$F = 1 + \frac{1}{G}\left\{\frac{T_2 N_2}{T_0 N_1} + \frac{T_3 N_3}{T_0 N_1} + \frac{T_4 N_4}{T_0 N_1}\right\}, \tag{50}$$

where G is the stage gain and N_2 is the relative noise contribution of the termination at port 2,

$$N_2 = \mathrm{Re}\left|\frac{1+\rho_2}{1-\rho_2}\right| \left| (\rho_1\rho_3 - 1)\left(\rho_3\frac{\rho_1-\rho_4}{2} - 1\right)^{-1}\left[\left(\frac{1}{2}\frac{(\rho_1+\rho_4)(\rho_1\rho_3-1)}{\rho_3\left(\frac{\rho_1-\rho_4}{2}\right)-1} - \rho_1\right)\left(1-\frac{1+\rho_2}{1-\rho_2}\right) + \frac{1+\rho_2}{1-\rho_2} + 1\right]^{-1}\right|^2 \tag{51}$$

N_1 is the relative noise contribution of the termination at port 3,

$$N_3 = \mathrm{Re}\left|\frac{1+\rho_3}{1-\rho_3}\right| \left| (\rho_1\rho_2 + 1)\left(\rho_2\frac{\rho_4-\rho_1}{2} - 1\right)^{-1}\left[\left(\frac{1}{2}\frac{(\rho_1+\rho_4)(\rho_2\rho_4+1)}{\rho_2\left(\frac{\rho_4-1}{2}\right)-1} + \rho_1\right)\left(1-\frac{1+\rho_3}{1-\rho_3}\right) + \frac{1+\rho_3}{1-\rho_3} + 1\right]^{-1}\right|^2 \tag{52}$$

N_4 is the relative noise contribution of the termination at port 4,

$$N_4 = 2\mathrm{Re}\left|\frac{1+\rho_4}{1-\rho_4}\right| \left| \frac{1+\frac{1+\rho_4}{1-\rho_4}}{\frac{\rho_2-\rho_3}{2} + \rho_1\left(\frac{\rho_2+\rho_3}{2}\right)^2\left(\rho_1\frac{\rho_2+\rho_3}{2}-1\right)^{-1} - \frac{1+\rho_4}{1-\rho_4} + 1}\right|^{-2} \tag{53}$$

N_1 is the relative noise contribution of the source at port 1,

$$N_1 = 2\,\mathrm{Re}\left|\frac{1+\rho_1}{1-\rho_1}\right| \left| \left(\frac{\rho_3+\rho_2}{2} + G\,\frac{\rho_4}{2}\right)\left(\rho_4\,\frac{\rho_2-\rho_3}{2} - 1\right)\left(1 - \frac{1+\rho_1}{1-\rho_1}\right) + \frac{1+\rho_1}{1-\rho_1} + 1 \right|^{-2} \tag{54}$$

when

$$\rho_2 = \rho_3 = \rho,$$
$$T_2 = T_3 = T,$$
$$\rho_4 = \rho_1 = 0,$$
$$T_4 = T_0, \text{ the ambient temperature.}$$

Equation (50) reduces to

$$F = 1 + \frac{T}{T_0}\left|\frac{1}{G} - 1\right|, \tag{55}$$

with $G = |\rho|^2$.

Typical Case

Using two parametric diodes with cutoff frequency $f_{co} = 75$ kmc, idler frequency $f_i = 10$ kmc, input frequency $f_s = 1$ kmc, $C_0 = 1$ picofarad and $\lambda V = 2/3$ picofarad, Equation (43) gives a negative resistance of

$$R = -\frac{1}{2\pi f_{co}}\,\frac{f_i}{f_s}\,\frac{C_0}{(\lambda V)^2} = -48 \text{ ohms.} \tag{56}$$

Hybrid junctions with 50-ohm characteristic impedance at ports 2 and 3 can easily be made. Large gains are therefore possible. If the stage gain is limited to 10 db, the stage noise figure is about ½ db.

Because the value of the negative resistance is low, the effect of the diode series resistance at the input is negligible. The effective noise temperature at ports 2 and 3 is therefore

$$T = T_0\,\frac{\omega_i}{\omega_0} = \frac{T_0}{10}. \tag{57}$$

If the noise figure of typical following stage is taken as 10 db, the overall noise figure is about 3 db. Note again that this stage must present a nearly perfect match over a band around the signal frequency to preserve stability and prevent additional noise figure deterioration.

The sensitivity of the amplifier to port termination is the major inconvenience of this solution. A strict control of the circuit is therefore necessary.

The above shortcomings can be traced to the bilaterality of the gain. A unilateral gain may however be obtained without resorting to expensive isolators or circulators. Solutions using ferrites in the idler circuit or controlling the phase of the pump signal on each diode[8-10] have been proposed.

Double-Sideband Parametric Amplifier

When the idler frequency is raised appreciably, the separation of the two modes by resonant circuits becomes very difficult. However, if the idler circuit has sufficient bandwidth, double-sideband amplification is possible.[11,12] The down-converter following the parametric amplifier must then also have sufficient input bandwidth.

The matrix (10) reduces to:

$$\begin{vmatrix} I_{\omega_0} \\ I_{\omega_s} \\ I_{\omega_i} \end{vmatrix} = \begin{vmatrix} j\omega_0 C_0 & j\omega_0 C_1 & j\omega_0 C_2 \\ j\omega_s C_1^* & j\omega_s C_0 & j\omega_s C_1 \\ j\omega_i C_2^* & j\omega_i C_1^* & j\omega_i C_0 \end{vmatrix} \begin{vmatrix} V_{\omega_0} \\ V_{\omega_s} \\ V_{\omega_i}^* \end{vmatrix} \tag{58}$$

where C_1 is basically the λV used above, and C_2 is a cross-coupling term between he sum $(\omega_0 = \omega_p + \omega_s)$ and the difference $(\omega_i = \omega_p - \omega_s)$ components. Only the sum (ω_0), difference (ω_i), pump (ω_p), and signal (ω_s) components are allowed to flow.

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[8] A. K. Kamel, "A Parametric Device as a Non-Reciprocal Element," *Proc. I.R.E.*, Vol. 38, p. 1424, Aug. 1950.

[9] L. D. Baldwin, "Non-Reciprocal Parametric Amplifier Circuit," *Proc. I.R.E.*, Vol. 49, p. 1075, June 1961.

[10] A. Korpel and P. Desmares, "Experiments with Nonreciprocal Parametric Devices," *Proc. I.R.E.*, Vol. 49, p. 1582, Oct. 1961.

[11] W. Eckhardt and F. Sterzer, "Microwave-Carrier Modulation–Demodulation Amplifiers and Logic Circuits," *Proc. I.R.E.*, Vol. 50, p. 148, Feb. 1962.

[12] W. Eckhardt and F. Sterzer, "Correction to Microwave-Carrier Modulation–Demodulation Amplifiers and Logic Circuits," *Proc. I.R.E.*, Vol. 50, p. 1632, July 1962.

Lossless parametric converter analysis shows that, for equal sideband loadings, zero net impedance is reflected at the input of the converter. Since a finite output is obtained for no net input power flow, an infinite gain is possible.

This can be visualized by considering Figure 20 which shows a dissected double-sideband amplifier. The signal flows in two sections: (1) a sum mode section where the signal is converted to $\omega_0 = \omega_p + \omega_s$, and a difference mode section where the signal is converted to $\omega_i = \omega_p - \omega_s$. For equal loadings at ω_s and ω_i, and under the assumption $\omega_{0,i} \gg \omega_s$, the sum-mode converter reflects a positive conductance G across the input while the difference mode converter reflects $-G$. The parallel combination is an infinite input impedance across which the source voltage is applied. The net power flow is zero, while both converters carry power which is down-converted coherently and appears at the output, yielding an infinite gain. Because the input impedance is capacitive, the gain–bandwidth product remains finite.

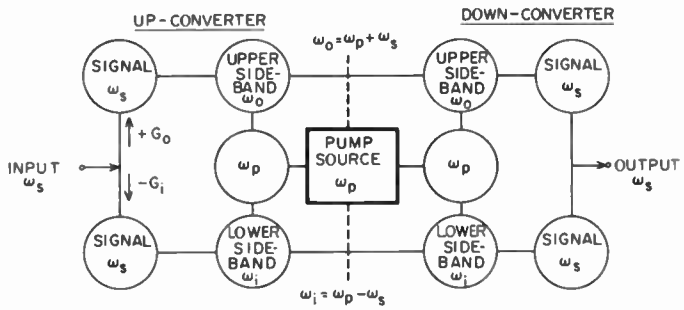

Fig. 20—Dissected double-sideband parametric up-converter followed by double-sideband crystal mixer down-converter.

The noise performance is evaluated by referring to Figure 21, which shows both input conductances $+G_0$ and $-G_i$. The associated equivalent current noise temperature to each conductance at the input is:

$$T_{0,i} = T_0 \frac{\omega_s}{\omega_{0,i}} \approx T_0 \frac{\omega_s}{\omega}, \tag{59}$$

$$\omega \approx \omega_0 \approx \omega_i.$$

The exchangeable noise power from each conductance is

$$<i_{0,i}>^2 = kT_0 B |G_{0,i}| \frac{\omega_s}{\omega}. \tag{60}$$

For a matched input

$$G_s = G_0 - G_i > 0; \tag{61}$$

the noise figure is then

$$F = 1 + \frac{\omega_s}{\omega} \frac{G_0 + G_i}{G_0 - G_i}, \tag{62}$$

$$G_0 > 0, \quad G_i > 0. \tag{62}$$

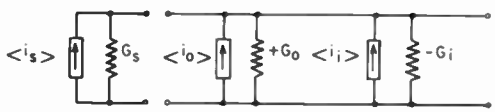

Fig. 21—Noise sources of double-sideband parametric amplifier.

The stage gain becomes

$$G = \frac{\omega}{\omega_s} \frac{G_0 + G_i}{G_0 - G_i}. \tag{63}$$

When the stage is followed by a down-converter with noise figure F_2, the over-all noise figure under matched condition is

$$F_{ov} = 1 + \frac{\omega_s}{\omega} \left\{ \frac{G_0 + G_i}{G_0 - G_i} + (F_2 - 1) \frac{G_0 - G_i}{G_0 + G_i} \right\}.$$

An optimum noise figure

$$F'_{ov} = 1 + \frac{\omega_s}{\omega} \left\{ \sqrt{F_2 - 1} + \frac{1}{\sqrt{F_2 - 1}} \right\}. \tag{65}$$

is obtained for

$$\frac{G_0 + G_i}{G_0 - G_i} = \sqrt{F_2 - 1}. \tag{66}$$

For a typical case of $F_2 = 10$ db and $\omega/\omega_s = 10$, the optimum over-all noise figure is below 1/2 db and the optimum gain is 30 db.

The results of the above simplified theory are altered by the diode and circuit losses. In most cases the input impedance can be made positive real, imaginary, or negative real by tilting the response at the output of the up-converter.

Double-sideband devices with a crystal mixer at a signal frequency of 1.2 kmc have been investigated. A voltage-gain–bandwidth of 70 mc and a noise figure below 3 db were reported.[11,12] The input match has been determined. The device is unilateral and can be cascaded with similar devices since the output impedance is positive real.

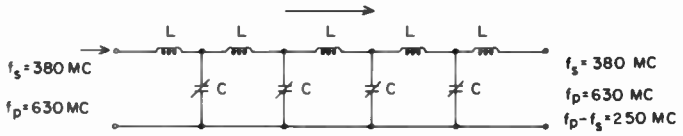

Fig. 22—Traveling-wave parametric amplifier.

Traveling-Wave Parametric Amplifier

When a series of parametric amplifiers are cascaded, the analysis of the device involves essentially a cascade of parametric networks such as those considered above. A signal and a pump are applied at one end of a transmission line having nonlinear reactances, and waves propagate away from this end to the other end, where the output circuit is usually located. The input signal generates signals at the sum and difference frequencies which propagate at different velocities along the dispersive line and amplification may occur in form of growing waves.[13,14]

A traveling-wave parametric amplifier of particularly simple structure is shown in Figure 22. Four parametric diodes were used, and the following results were observed:

Signal frequency	:	380 mc;
Pump frequency	:	630 mc;
Idler frequency	:	250 mc

[13] P. K. Tien and H. Suhl, "Traveling-Wave Ferromagnetic Amplifier," *Proc. I.R.E.*, Vol. 46, p. 701, April 1958.

[14] R. S. Englebrecht, "A Low-Noise–Linear-Reactance Traveling-Wave Amplifier," *Proc. I.R.E.*, Vol. 46, p. 1655, Sept. 1958.

Forward-signal gain	:	10-12 db
Conversion gain (380 to 250 mc)	:	8-10 db
Bandwidth	:	10-20 mc
Noise figure	:	3.5 db
Match	:	Not established.

The need for a large number of diodes is a distinct disadvantage for application to television receivers. Transmission lines uniformly loaded by evaporated parametric diodes could lower the cost, but this technique is not within the present state of the art.

Summary and Conclusion

Some salient characteristics of various forms of junction-diode parametric amplifier have been determined. Experimental results with sum-mode parametric amplifiers were found to agree with the predicted results. The noise figure of two embodiments of particular interest in the television-receiver field have been evaluated over a wide range of design parameters of practical interest. The noise figure was found to vary from 2.7 to 7.7 db for imbedded preamplifiers and from 6.2 to 12.5 db for autonomous preamplifiers. There is, therefore, a large benefit in the use the imbedded preamplifier version despite its greater complexity.

The stability of difference-mode parametric amplifiers has been analyzed. Immunity from source impedance variation can be achieved with hybrid junction embodiments. The importance of accurate terminations at ports 2, 3 and 4 has been established. The dependence of the noise figure on the termination at all the hybrid junction ports has been shown, and an over-all noise figure of 3 db is found possible with parametric stage gain as low as 10 db. The gain of the difference mode amplifier is not limited to the output–input frequency ratio, and better noise figures are therefore possible.

A double-sideband parametric amplifier without loss has been analyzed and was shown to require an appropriate tilting in the up-converter circuit response to yield an input match and good noise figure.

A major inconvenience, shared by all parametric amplifiers, is their requirement of a pump with frequency much above the input frequency. An estimated power of 50 to 100 milliwatts at 10 kmc is

judged necessary for a parametric amplifier operational in television receivers. Tunnel diodes may be able to furnish this power at a reasonable cost. However, this power range is one to two orders of magnitude above the present state of the art.[15,16]

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[15] F. Sterzer and D. E. Nelson, "Tunnel Diode Microwave Oscillator," *Proc. I.R.E.*, Vol. 49, p. 744, April 1961.

[16] E. Johnson, "The Tunnel Diode: Can It Compete?," *Electronic Design*, p. 37, May 24, 1962.

AN EXPERIMENTAL PARAMETRIC TUNER FOR UHF TELEVISION RECEIVERS

By

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Summary—A parametric tuner has been developed and its feasibility for television receivers investigated. The tuner operates in a sum-mode configuration and exhibits a noise figure of 4 db at 575 mc. Further reduction of the noise figure can be expected with improved varactor diodes. The tuner is designed to operate in the VHF and UHF television bands. Manufacturing cost and simplicity are considered. It is shown that the feasibility of a parametric tuner depends on the availability of a low-cost microwave pump. This pump should preferably be a solid-state device such as a tunnel diode. At present, tunnel diodes are capable of operating at very high frequencies, but the power output in X-band is insufficient. Furthermore, means to tune and stabilize high-frequency (X-band) oscillators are not at hand.

Introduction

RECENT DEVELOPMENTS of parametric devices for low-signal-level amplification have opened a new avenue of approach to the design of UHF tuners. At present, the performance of UHF tuners is inferior to that of VHF tuners with regard to noise figure and other characteristics. Although inexpensive mass-produced vacuum tubes perform adequately in the VHF range, they provide little improvement in performance at UHF. UHF tubes which have the necessary performance are expensive mainly because of their critical geometry. Transistors are available that have noise performance characteristics comparable to those of tubes in the VHF–UHF range. However, their ultimate noise performance is inferior to that of parametric amplifiers.

Parametric amplifiers that are already in use and are available on the market exhibit noise figures considerably lower than can be expected with either tubes or transistors; however, they are unsuitable for use in television receivers at the present time because of price, critical operation, size and other factors. This paper considers the possibility of designing parametric amplifiers that would be practical for use in television receivers.

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Of the several possible modes of parametric operation, the sum-mode is preferred for a television tuner, because it is the only mode where the gain stability is independent of the antenna termination. Practical circulators operating in the VHF and UHF bands are not available at the present time and this limits further consideration of the negative-resistance type of parametric amplifier.

The analysis of the sum-mode up-converter given below predicts a relatively low noise figure, but also reveals that considerable pump power is required to energize the varactor diode. A parametric tuner consisting of an up-converter and down-converter, together with a klystron pump and UHF oscillator circuits, is described in detail. A klystron and a UHF oscillator were utilized because tunnel diode oscillators with sufficient power were not available at the time. The performance of the parametric tuner is evaluated and the results are compared with theoretical calculations.

Although the noise figure obtained with varactor diodes now available is lower than is possible with any other current technique, it seems that improved diodes could produce still better results. Further development of the parametric tuner depends on the availability of a suitable high-frequency pump.

System Considerations

In general, parametric systems can be classified into three basic types: (1) the sum-mode up-converter; (2) the difference-mode up-converter; and (3) the negative-resistance amplifier.

In the sum-mode up-converter, the output frequency is equal to the sum of the signal frequency and the pump frequency; power flow at other than the above frequencies is negligible. Theoretically, a sum-mode up-converter should be absolutely stable, even with improper termination of the input and output terminals. The maximum possible power gain with this configuration is equal to the ratio of the output frequency to the input frequency.

In the difference-mode up-converter, the output frequency is equal to the difference between the pump frequency and signal frequency. This system presents negative resistance and requires stabilization at both input and output terminals to prevent oscillation. If the output is taken at the sum frequency, while a certain amount of power at the difference frequency is allowed to be present, a combination of the sum-mode and difference-mode up-converter is obtained and the device is potentially unstable.

In the negative-resistance parametric amplifier, the output frequency is equal to the input frequency. As in the difference-mode up-

converter, the negative-resistance amplifier requires stabilization. Also, there is a significant amount of power flow at a frequency corresponding to the difference between the pump and signal frequencies. There are two types of negative-resistance amplifiers. They are distinguished by the operating frequency of the pump relative to the signal frequency. In the degenerate amplifier, the pump frequency is twice the signal frequency, while in the nondegenerate amplifier the pump frequency, while higher than the signal frequency, is of arbitrary value.

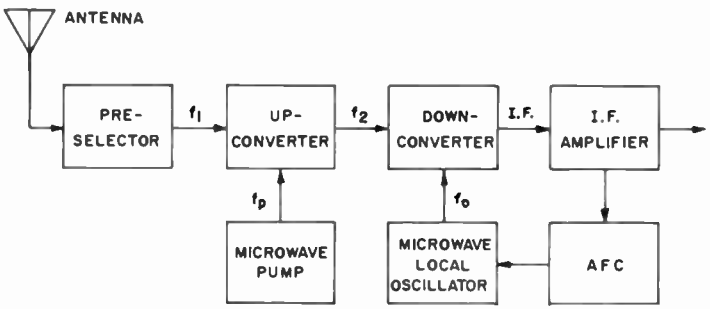

Fig. 1—Parametric tuner system using two microwave sources.

Even though the available gain of both the difference-mode up-converter and the negative-resistance amplifier is greater than that obtained with the sum-mode up-converter (so that lower over-all system noise figure is possible), stable operation with these negative-resistance systems requires the use of circulators or other means[1] to provide proper termination in order to prevent oscillation. For application in a VHF–UHF television tuner where the antenna termination can vary drastically, the negative-resistance systems appear to be impractical at present.

This leads to the choice of the sum-mode up-converter for use in the parametric television tuner.

Parametric Television Tuner Configurations

A block diagram of a television tuner using a parametric up-converter is shown in Figure 1. In this system, the input signal from the receiving antenna, at frequency f_1, is coupled to a varactor diode in the up-converter by means of tunable pre-selector circuits. The varactor diode is also energized by the microwave pump signal, at

[1] D. d'Agostini, "The Performance of Sum and Difference Mode Parametric Amplifiers in Television Receivers," *RCA Review*, Vol. XXIV, p. 226, June 1963.

frequency f_p, and the resulting idler signal, $f_1 + f_p$, is applied to the down-converter. The i-f output signal is obtained by heterodyning the idler frequency with the microwave local oscillator at frequency $f_1 + f_p$ + i-f. The automatic-frequency-control circuit provides compensation for frequency drift in the local oscillator of the down-converter. In this system, the pump frequency is tuned in accordance with the desired signal to keep the idler frequency constant.

To obtain reasonable gain at the highest signal frequency (890 mc), a 9.5 gc (gigacycle = 10^9 cycles) idler frequency is used. This

Table I—Pump frequencies for a parametric television tuner (picture i-f = 45.75 mc; idler frequency = 9500 mc; down-converter local oscillator frequency = 9545.75 mc).

Channel	Picture Carrier Frequency	Pump Frequency
Low Band		
2	55.25	944.75
6	83.25	9416.75
High Band		
7	175.25	9324.75
13	211.25	9288.75
UHF		
14	471.25	9028.75
83	885.25	9614.75

requires both the pump and down-converter local oscillator to operate in the X-band frequency range. The respective oscillators should be capable of delivering required power, and should be sufficiently stable to maintain the idler signal within the passband of the idler circuit. Only one of the oscillators requires frequency compensation, and the down-converter local oscillator was chosen because less power output will be required from this oscillator. The frequencies of the pump for the VHF and UHF television channels are given in Table I.

An alternative tuner system using a single microwave source is shown in Figure 2. Here, as in the previously described system, the input signal from the antenna is coupled to the varactor diode by means of the pre-selector circuit. However, the pump signal is derived by mixing the signals of two oscillators—a fixed high-frequency oscillator (microwave local oscillator) and a variable low-frequency oscillator (VHF-UHF local oscillator). These signals are coupled to a mixer

and the resulting sum frequency is applied to the varactor diode in the up-converter. The fixed-frequency oscillator also energizes the down-converter diode where the idler frequency signal is converted to i-f. With a 9.5 gc idler frequency, the frequency of the fixed tuned oscillator is 9.545 gc and the frequency of the lower-frequency oscillator varies with f_1. Reasonable frequency stability can be expected of this system, since stability is determined by the low-frequency oscillator, which has a tuning range identical with that employed in present commercial VHF and UHF tuners.

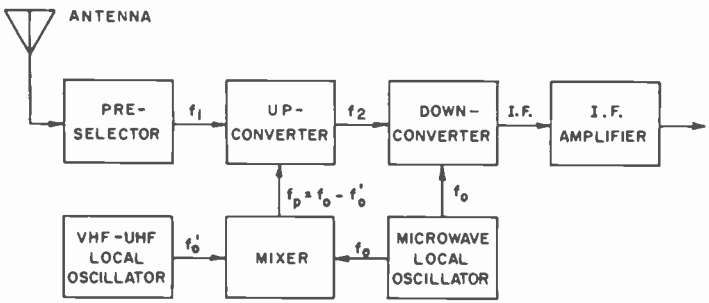

Fig. 2—Parametric tuner system using a single microwave source.

A serious problem in the above system is the presence of interfering signals generated in the mixer as a result of harmonics of the low-frequency oscillator. In addition, the available power from the microwave oscillator must be sufficient to compensate for the loss in the mixer. Because of the above problems, the first of the two systems described appears to be the more desirable.

In the experimental setup, the high-frequency oscillator, a klystron tube, was coupled to the varactor diode and the derived signal generated in the mixer was applied to the down-converter diode. The microwave frequencies were chosen so that spurious responses were avoided.

The practicability of either of the two tuner systems described depends on the availability of low-cost microwave oscillators of adequate power. Solid-state oscillators using a tunnel diode as the active device are capable of operating in the desired frequency range, but at the present time their power output is only a fraction of a milliwatt. It can be expected that tunnel diodes will be improved in this respect.

Theoretical Performance

Up-converter Performance

Since the theory of the upper-sideband parametric up-converter

(sum mode) is adequately covered in the literature,[2,3] the treatment here is limited to the application of the theory to the up-converter used in the parametric television tuner. Due to the relatively high second-stage noise figure, the system under consideration will have a minimum over-all noise figure when the first-stage gain is at a maximum. Therefore, only the maximum-gain condition is considered here.

The over-all up-converter performance is determined by the dynamic quality factor of the diode and the input-to-output frequency ratio. As defined by Uenohara,[4] the dynamic quality factor is

$$\tilde{Q} = \frac{Q}{\frac{2C_0}{C_1} - \frac{C_1}{2C_0}}, \tag{1}$$

where C_0 is the first term and C_1 the coefficient of the first dynamic term of the Fourier expansion of the capacitance–voltage characteristic of the varactor diode. C_0 corresponds to the static capacitance of the diode at the operating point. The quality factor Q is defined as

$$Q = \frac{1}{\omega C_0 R_s}, \tag{2}$$

where ω is the angular frequency and R_s the spreading resistance of the varactor diode. It is convenient to define the quantity

$$\gamma = \frac{C_1}{C_0}, \tag{2}$$

which is the ratio of fundamental to static capacitance. This quantity is a function of the pump power applied to the varactor diode and is a key factor in the determination of parametric-amplifier and up-converter performance. In terms of γ and the signal and idler frequencies, f_1 and f_2, the maximum gain for the sum-mode up-converter has been shown to be[3]

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[2] L. A. Blackwell and K. L. Kotzebue, *Semiconductor-Diode Parametric Amplifiers*, Prentice-Hall, Inc., Englewood Cliffs, N. J., 1961.

[3] K. Kurokawa and M. Uenohara, "Minimum Noise Figure of the Variable-Capacitance Amplifier," *Bell Syst. Tech. Jour.*, Vol. 40, No. 3, p. 714, May 1961.

[4] M. Uenohara and H. Seidel, "961-mc Lower-Sideband Up-Converter for Satellite-Tracking Radar," *Bell Syst. Tech. Jour.*, Vol. 40, No. 4, p. 1189, July 1961.

$$G = \frac{f_2}{f_1}\frac{K-1}{K+1}, \tag{3}$$

where

$$K = \left[1 + \left(\frac{f_1}{f_2}\right)\tilde{Q}_1^2\right]^{1/2},$$

$$\tilde{Q}_1 = \frac{Q_1}{\frac{2}{\gamma} - \frac{\gamma}{2}},$$

$$Q_1 = \frac{1}{\omega_1 C_0 R_s}.$$

The gain given by Equation (3) is less than the output-to-input frequency ratio due to the diode losses and the limited fundamental capacitance variation. As the dynamic quality factor increases, the gain approaches the frequency ratio f_2/f_1.

Under the maximum-gain condition, the noise figure for the up-converter is given by[3]

$$F = 1 + \frac{1}{K}\left(1 + \frac{f_1}{f_2}\frac{K+1}{K-1}\right), \tag{4}$$

or, in terms of the gain,

$$F = 1 + \frac{1}{K}\left(1 + \frac{1}{G}\right). \tag{5}$$

As the dynamic quality factor of the diode is increased, the noise figure is decreased, so that as the gain approaches the frequency ratio f_2/f_1, the noise figure tends toward unity, or zero db.

A plot of the maximum gain of the upper-sideband up-converter as a function of the dynamic quality factor for several different output to input frequency ratios is shown in Figure 3. The corresponding set of curves for the noise figure is shown in Figure 4. The frequency ratio for the system under consideration varies from 10.5 to 175, assuming an idler frequency of 9.5 gc. For commercially available varactor diodes, the dynamic quality factor roughly encompasses the values 15 to 200 for frequencies in the VHF-UHF range.

The up-converter performance as a function of frequency and γ is indicated more clearly in Figure 5, which shows the variation of the

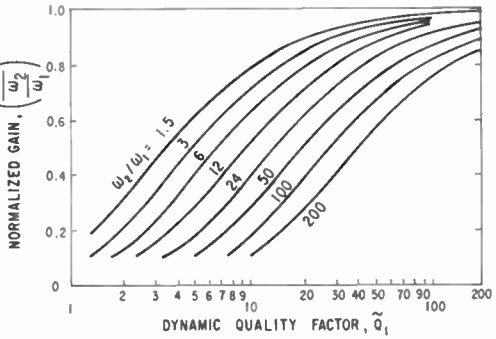


Fig. 3—Normalized maximum gain of upper-sideband up-converter.

maximum gain over the VHF-UHF range for several values of γ. In this case, the idler frequency was chosen as 9.5 gc and the diode cutoff frequency 50 gc ($f_c = 1/(2\pi C_j R_s)$). A similar plot for the noise figure is shown in Figure 6. These curves indicate satisfactory gain and noise figure for the conditions assumed.

System Noise Performance

The system noise figure of the parametric tuner can be expressed as

$$F = F_1 + \frac{F_2 - 1}{G_1}, \tag{6}$$

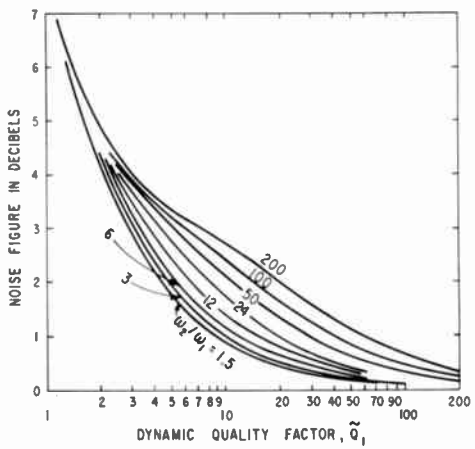


Fig. 4—Noise figure of upper-sideband up-converter under maximum-gain condition.

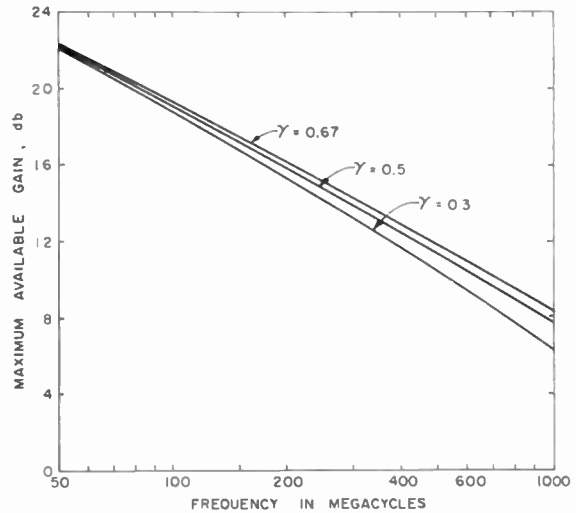


Fig. 5—Maximum gain of sum-mode up-converter.

where F_1 is the up-converter noise figure, G_1 is the up-converter gain, and F_2 is the down-converter noise figure. Assuming ideal conditions, where the dynamic Q of the varactor diode is sufficiently high so that the gain is equal to the output-to-input frequency ratio and the noise figure of the up-converter is unity, the minimum over-all noise figure will be

$$F = 1 + \frac{f_2}{f_1}(F_2 - 1). \tag{7}$$

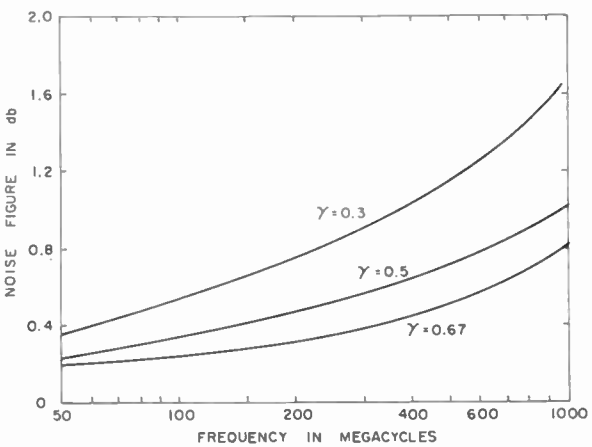


Fig. 6—Sum-mode up-converter noise figure.

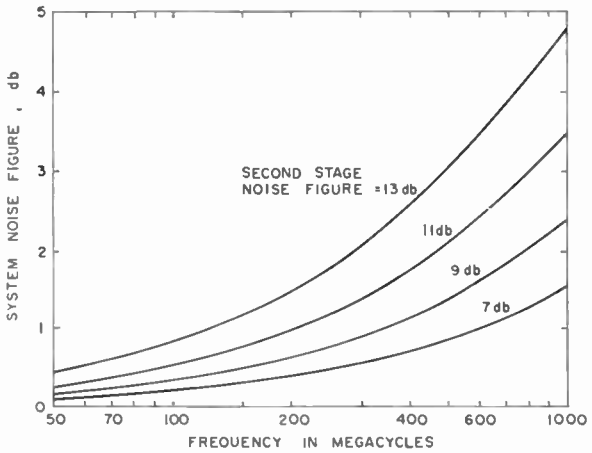


Fig. 7—Over-all noise figure of ideal sum-mode parametric up-converter.

System noise figure as a function of signal frequency (Equation (7)) has been plotted in Figure 7 for several different second-stage noise figures. It is evident from the over-all noise-figure curves of Figure 7 that due to limited available gain, the noise contributed by the down-converter is significant even for the ideal sum-mode up-converter. Using the up-converter gain and noise figure obtained from Equations (3) and (5), the over-all system noise figure varies over the VHF-UHF band as shown in Figure 8. Curves for several different

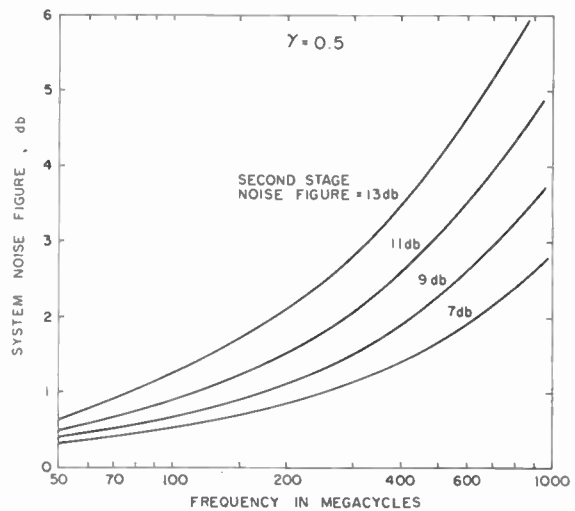


Fig. 8—Over-all system noise figure of sum-mode up-converter followed by down-converter.

second-stage noise figures are plotted using a value of 0.5 for γ. A similar set of curves are shown in Figure 9 for $\gamma = 0.3$. A practical value of γ for commercially available diodes with moderate pumping is between 0.3 and 0.5.

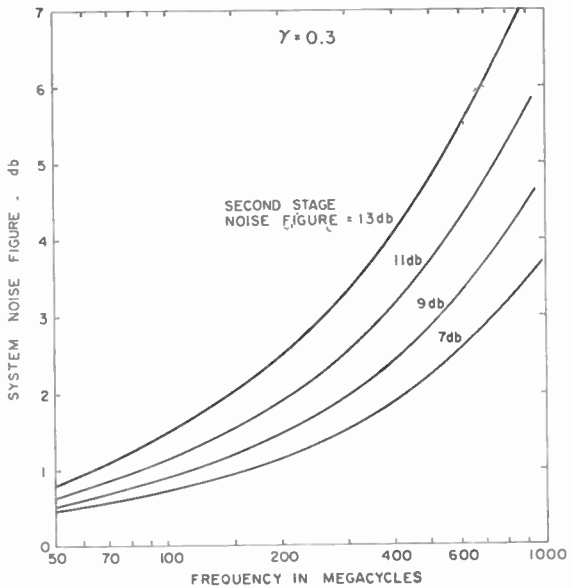


Fig. 9—Over-all system noise figure of sum-mode up-converter followed by down-converter.

Effect of Circuit Losses

The gain and noise figure discussed above do not include the effect of circuit loss and bandwidth in the various parts of the parametric tuner. At microwave frequencies, the circuit loss and bandwidth of the pump and idler circuits influence the up-converter performance. An even more significant effect on tuner performance is the insertion loss produced by the pre-selector circuits at the signal frequency. The effects at the input are more pronounced than at the output of the up-converter, since the noise figure is a direct function of the insertion loss at the input. At the output, effects of idler frequency losses are somewhat masked by the gain of the up-converter.

Pump and Idler Circuit Losses

Circuit losses due to the circuits which are tuned to the pump frequency can be overcome by additional pump power. However, these

losses cannot be cancelled at the idler frequency, and the bandwidth and Q of the idler circuit will affect the over-all tuner performance. The idler-circuit bandwidth depends upon the loading provided by the varactor diode and also upon the coupling of the idler circuit to the down-converter. In the up-converter system utilizing a derived local oscillator signal for the down-converter, the idler-circuit bandwidth must be broad enough that the frequency drift of the microwave pump oscillator does not cause the idler frequency to pass out of its passband. Also, the selectivity provided by the idler and input pre-selector circuits must be such that adequate attenuation is provided for the image signal. The insertion loss, L, of a tuned circuit in terms of the loaded and unloaded circuit Q's is expressed as[5]

$$L \doteq 20 \log_{10} \left(1 + \frac{Q_L}{Q_0} \right) \text{db} \tag{8}$$

where Q_L is the loaded Q of the circuit and Q_0 is the unloaded Q of the circuit.

Unloaded circuit Q's in the order of 3000 to 3500 are readily available with capacitance-tuned resonant cavities. A bandwidth of 20 mc for the idler circuit results in a loaded Q of 475 for an idler frequency of 9.5 gc. The corresponding insertion loss for such a system would be 0.6 db. Since the insertion loss in the idler circuit occurs after amplification of the signal, its effect can be considered equivalent to a poorer second-stage noise figure. Thus, the noise figure of the up-converter is not appreciably deteriorated by losses in the idler circuit.

Input Circuit Losses

The insertion losses in the input are due primarily to the circuit losses and to the impedance mismatch between the input and the antenna. At VHF, the input losses represent a large portion of the over-all system noise; however, since the up-conversion process for this frequency range is so efficient, the over-all system noise figure will still be quite low (< 3 db). These losses also add to the system noise in the UHF range, but at these frequencies the up-converter performance is not as good as at VHF, so that the effect of the added losses is more serious.

At UHF, circuit Q's between 500 and 1000 are obtainable using a capacitively tuned section of line. With a 3-db bandwidth of 20 mc,

[5] G. L. Ragan, *Microwave Transmission Circuit*, McGraw-Hill Book Company, Inc., New York, 1948, p. 654.

the ohmic power loss is in the order of 0.25 db. Allowing for a 2 to 1 voltage-standing-wave ratio at the input due to tracking errors and impedance mismatch, the total insertion loss due to this cause is 0.5 db. The total theoretical input loss would be between 0.5 and 1 db for the conditions assumed above. This loss should be added to the curves of Figures 8 and 9 to obtain the theoretical system noise figure with the effects of circuit loss and mismatch included.

Reverse Current Induced Noise[6]

To obtain optimum performance from the parametric up-converter, the capacitance of the varactor diode must be swept over its entire range. The maximum swing is determined by the point at which the diode is driven into forward conduction and the point at which reverse breakdown occurs. Significant deterioration of the noise figure of the up-converter occurs when a current as low as 5 microamperes is drawn in the reverse direction. The reverse-current noise is found to increase as the ratio f_c/F_D increases, where f_c is the cutoff frequency of the diode and F_D the noise figure of the parametric amplifier using the diode. Thus for a given breakdown voltage, the better diodes produce the most reverse-current noise.

Since the reverse current induces noise, the useful maximum excursion of the capacitance swing is limited to the region where no appreciable reverse current flows. For this reason, it is not feasible to pump the varactor diode to the point where optimum gain is obtained. If the gain of the up-converter is limited, more noise is contributed from the relatively noisy down-converter which follows it. The noise introduced by the reverse current is one of the more serious limitations imposed on the gain and noise figure of the sum-mode up-converter.

Pump Power Requirements

In a parametric amplifier or up-converter, the varactor diode is driven from a high-frequency source (the pump) to produce the time-varying capacitance necessary for signal amplification. It is of interest to know the magnitude of this pump power as a function of the characteristic parameters and operating conditions of the varactor diode. The pump power is utilized in the amplification process and is dissipated for the most part in the diode series resistance.

A simplified equivalent circuit of the varactor diode consists of a voltage-dependent junction capacitance C, in series with the bulk or

[6] R. D. Weglein, "Some Limitations on Parametric Amplifier Noise Performance," *Trans. I.R.E. PGMTT*, Vol. MTT 8, No. 5, p. 538, September 1960.

spreading resistance R_s. The resistance R_s is of the order of a few ohms and is almost independent of frequency and the applied bias. If the voltage E represents the r-m-s value of the pump voltage across the junction capacitance, the resultant current, I, in this capacitance is $j\omega CE$. Since this current is also common with the series resistance R_s, the power dissipated in R_s will be

$$I^2R_s = E^2\omega^2C^2R_s. \tag{9}$$

In terms of the cutoff frequency, $f_c = 1/(2\pi R_sC)$, the power dissipated can be expressed as

$$P = \frac{2\pi CE^2f^2}{f_c}. \tag{10}$$

In Equations (9) and (10), the capacitance C has been assumed to be the capacitance at the operating point. For a diode such as the MA450F, the cutoff frequency referred to the operating point is about 50 gc, and the operating capacitance is approximately 1 micromicrofarad. Assuming that 1.5 volts r-m-s of pump voltage is required to produce the desired capacitance variation, the power required at 9.5 gc is 11.5 milliwatts. Equation (10) gives only a rough indication of the actual power required, since the capacitance C is nonlinear and the voltage E across the junction has been only an estimate.

Development of the Tuner

The preselector circuits must cover the entire VHF–UHF range of 54 to 980 mc. Since noise figure was not considered a serious problem in the VHF range, the effort in this work was concentrated in the UHF range. In the proposed system, the input circuit would be capacitively tuned; a band switch is used to insert the appropriate inductance in series with the capacitance. A schematic diagram of such a circuit is shown in Figure 10. Two resonant circuits are used in the input to obtain the necessary image attenuation, with a 3-db bandwidth in the VHF range of approximately 6 mc. In the UHF range the input bandwidth would be about 20 mc, as previously mentioned, to keep the input insertion loss low. In most respects the techniques that are presently being used in the input circuit of VHF and UHF television tuners may be applied to the design of the input circuits for the parametric tuner.

The resonant circuit element used for the up-converter and down-converter will, to a large extent, determine the structural configuration

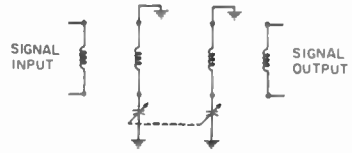


Fig. 10—Preselector circuit with band switching.

of the parametric television tuner. The choice of a particular microwave tuning means for the parametric up-converter is governed by practical and economic considerations. The construction should be adaptable for mass production at low cost, and at the same time it should be reliable in operation and easy to align. Transmission lines (such as the stripline) are relatively easy to manufacture, but tuning over a given microwave frequency range presents a mechanical problem. Tunable waveguide lines are not practical because of their large size and difficulty in tuning and assembly. The use of the capacitance-tuned microwave cavity appears to be a more-reasonable approach for the parametric tuner.

Of all the various microwave cavities, the rectangular cavity, besides fulfilling the size and electrical characteristic requirements, is the simplest to manufacture. The mechanical structure of the cavity with provision for tuning is shown in Figure 11(a). Electric and magnetic fields corresponding to the TE_{101} mode are shown in Figure 11(b).

For a rectangular cavity such as that shown in Figure 11(a), the resonant wavelength, neglecting the capacitance screw, is[7]

$$\lambda_1 = \frac{2ad}{(a^2 + d^2)^{1/2}} \tag{11}$$

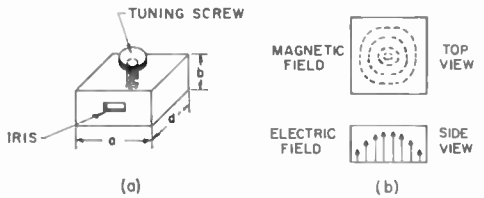


Fig. 11—Resonant cavity with corresponding fields for TE_{101} mode of operation.

[7] S. Ramo and J. R. Whinnery, *Fields and Waves in Modern Radio*, John Wiley and Sons, New York, 1944, p. 385.

where a and d are the length and width of the box, as shown in Figure 11(a). When the cavity is a square prism with $a = d$, the wavelength becomes $a\sqrt{2}$. The corresponding unloaded Q for the rectangular cavity is[8]

$$Q = \frac{\pi\eta_1}{4R_s} \frac{(a^2 + d^2)^{3/2}}{a^3 + d^3 + \frac{ad}{2b}(a^2 + d^2)}, \tag{12}$$

where $\eta_1 =$ intrinsic impedance $= 120\pi$ ohms,

$R_s =$ skin-effect surface resistivity $= 2.61 \times 10^{-7}\sqrt{f}$ for copper and $5.01 \times 10^{-7}\sqrt{f}$ for brass.

A rectangular cavity with the inside dimensions of $a = 0.9$ inch, $d = 0.7$ inch and $b = 0.4$ inch has a resonant frequency of 10.7 gc. Using copper as the cavity material, an unloaded Q of 7760 is obtained at this frequency. When brass is used, the corresponding Q is found to be 4050. Additional circuit losses are introduced by the capacitance tuning screw so that the effective Q is between 3000 and 4000. A tuning range of approximately 1.4 gc at 10 gc, can be obtained by the use of a capacitive tuning screw. This is more than adequate to cover the tuning range of the high-frequency pump required for the television spectrum.

The microwave coupling to the resonant cavity was accomplished by use of a predominantly inductive iris as illustrated in Figure 11(a). These irises were used to couple the pump energy into the pump cavity and also to couple the idler energy out of the idler-circuit cavity. It was found that an iris 5/16 by 5/32 inch gave the desired coupling to the cavity when an iris thickness of 1/16 inch was used.

Since only partial loading of the resonant cavity by either the varactor diode or the point-contact diode is desired, it is necessary to tap the diodes down on the microwave resonant circuit. One method of decoupling the diode from the cavity is to place the diode close to one of the sidewalls of the cavity. This method was used in both the up-converter and down-converter described.

Signal frequencies in the 54 to 980 mc frequency range were coupled to the varactor diode by use of the microwave filter shown in Figure 12. This filter consists basically of an open-circuited 3/4-wave radial transmission line which presents a short circuit for microwave frequencies but behaves as a small capacitance for signal frequencies.

[8] See Reference (6), p. 390.

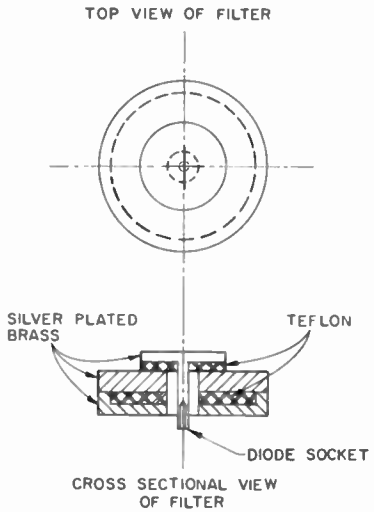


Fig. 12—Microwave filter.

An input filter of simpler design consisting of a quarter-wave radial line was used in some of the up-converters. However, for unconditionally stable parametric operation, the more-complex input microwave filter of Figure 12 was found to be a necessity because difference-mode resonances would occur in the input circuit if the radial line were used.

The up-converter incorporates two of the microwave resonant cavities previously described placed adjacent to one another as shown in Figure 13. One cavity is used in the pump circuit and the other for the sum-mode idler circuit. Decoupling of the varactor diode from both

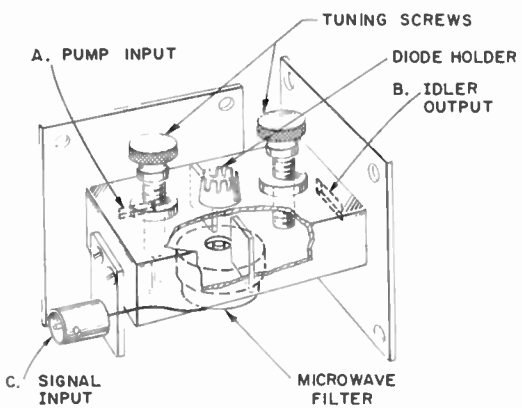


Fig. 13—Up-converter structure.

cavities is accomplished by placing the diode in the center of the partition wall between the two resonant cavities as illustrated in Figure 13.

The varactor diode is held between the crown shown on the upper side of the up-converter structure and the microwave filter assembly on the bottom of the structure. Irises A and B provide the means to couple the pump oscillator into the pump cavity and the idler signal out of the idler cavity. The input signal at VHF or UHF from the pre-selector is applied to the up-converter at terminal C, which is connected to the varactor diode through the microwave input filter.

Tuning of the microwave cavities is achieved by means of the capacitive tuning screws centrally located in each of the cavities as shown

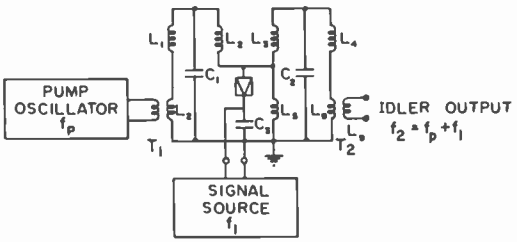


Fig. 14—Circuit diagram of the up-converter.

in Figure 13. In the complete tuner, for a variable signal frequency input, the pump-tuning screw must be made to vary in accord with the signal so that the idler frequency is kept constant. Since the pump frequency is always lower than the idler frequency, the pump cavity is made slightly larger (.4 × .9 × .8 inch) than the idler-circuit cavity (.4 × .9 × .7 inch). Thus the capacitance added by the tuning screw is kept to a minimum to reduce circuit loss.

An equivalent circuit of the up-converter is shown in Figure 14. Here, the pump-circuit resonant cavity is comprised of the inductances L_1, L_2 and the capacitance C_1, while the transformer T_1 represents the iris for this cavity. Similarly, the inductances L_3 and L_4 and the capacitance C_2 comprise the equivalent circuit for the idler-cavity resonator, with the transformer T_2 representing the idler output-coupling iris. The varactor diode is shunted by the inductance L_5 which is equivalent to the iris between the two resonators. Capacitance C_3 provides a short at microwave frequencies and is also the input capacitance at the signal frequency. In the more-complex input-filter structure, C_3 would represent the 3/4-wave radial transmission line.

As shown in Figure 15, the down-converter is quite similar in structure to the up-converter. The main differences are the use of the simpler quarter-wave filter for the microwave bypass and i-f output and the symmetrical resonant cavities (each $.4 \times .9 \times .7$ inches) used in the down-converter local oscillator. Output at the intermediate frequency is taken from the F terminal.

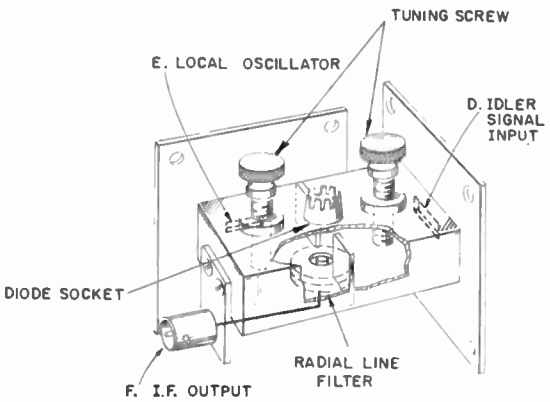
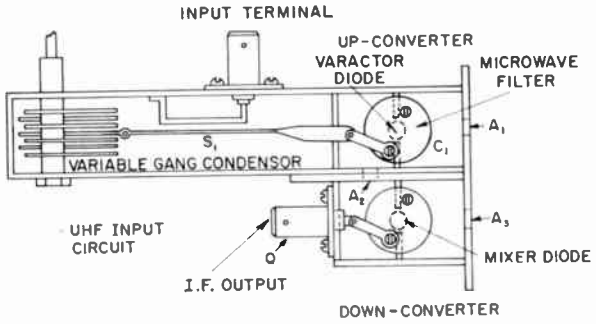


Fig. 15—Down-converter structure.

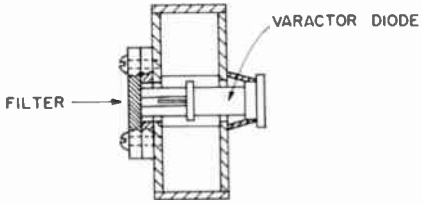
The equivalent circuit of the down-converter does not differ materially from that of the up-converter and is shown in detail in Figure 17 as part of the complete tuner circuit.

The complete tuner structure, consisting of the pre-selector, up-converter, and down-converter, is assembled as shown in Figure 16. In this assembly, the output from the pre-selector circuit S_1 is fed to the varactor diode through the microwave bypass capacitor C_1. The pump oscillator is fed to the diode through the aperture A_1 of the up-converter, and the sum-mode idler signal resulting from the mixing of the signal and pump oscillator is coupled to the down-converter through the iris A_2. Local oscillator excitation of the point-contact diode in the down-converter is made through the aperture A_3, and the i-f resulting from the mixing of the local oscillator and idler signal is taken out from terminal Q. The circuit diagram of the parametric tuning unit is shown in Figure 17. The broken lines indicate the pre-selector, up-converter, and down-converter portions of the tuner.

Although Figure 17 shows only the UHF pre-selector circuits, the VHF circuits would normally be included by use of a switching mechanism. The main power source at microwave frequencies used in this tuner has been an X-13 klystron; the other required microwave signals are derived by a mixing process.



a. SECTIONAL VIEW



b. DIODE MOUNT

Fig. 16—Parametric tuner.

Experimental Results

Since the main purpose of this investigation was to determine the feasibility of a low-noise parametric system for UHF television application, the main effort was directed towards obtaining optimum performance in this frequency range. To this end, the noise figure and gain measurements were made in the UHF range.

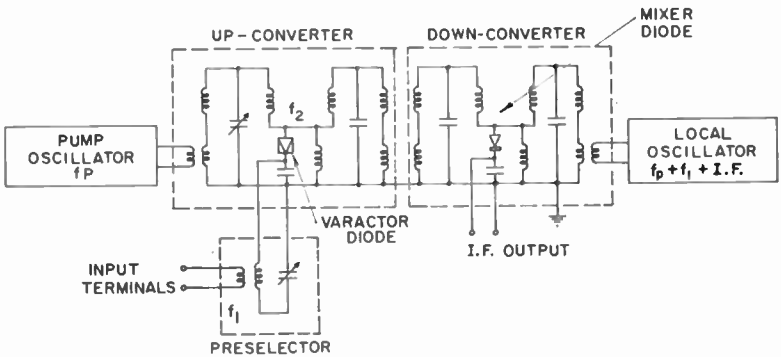


Fig. 17—Circuit diagram of the parametric tuner.

Noise Figure and Gain Characteristic of Tuner

The performance of the parametric tuner depends to a great extent on the first-stage noise figure and gain. These, in turn, are functions of the output-to-input frequency ratio, the pump power applied to the diode, and the characteristic of the varactor diode used.

The measured values of the up-converter noise figure as a function of the pump power applied to the diode are shown by curve A of Figure 18. For these measurements, an MA450F varactor diode was used at

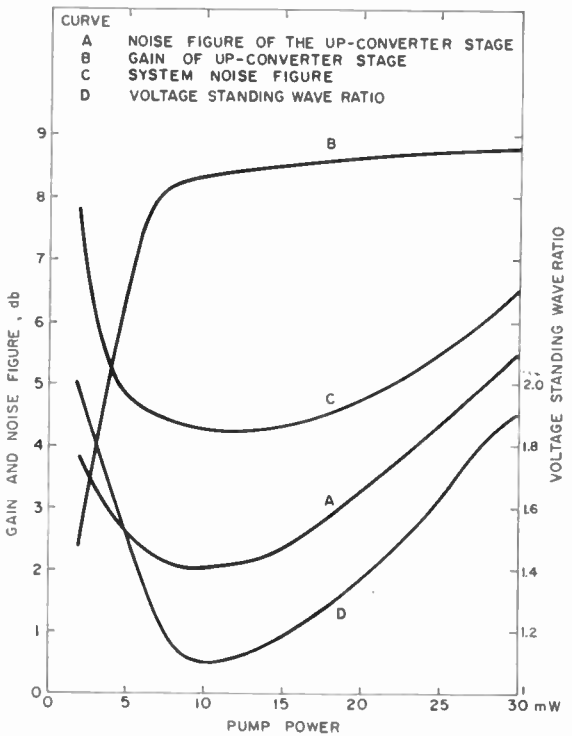


Fig. 18—Gain and noise figure of the up-converter with a MA450F varactor diode. ($V_{BR} = 6$ volts)

a signal frequency of 575 mc. The corresponding up-converter gain measured by the bolometer method is shown by curve B of Figure 18. The input circuit losses have been deducted so that the noise figure shown represents the up-converter noise alone. It is noted that the noise figure of the up-converter increases as the pump power is increased above 10 mw, while the gain of the stage increases sharply up to a pump power of about 8 mw and then levels off. Since the over-all

system noise figure is dependent upon both the gain and noise figure of the first stage, the minimum system noise figure occurs at a different level of pump power than that required to obtain minimum first-stage noise figure. Using a second-stage down-converter with a noise figure of 8.7 db, the measured over-all system noise figure shown by curve C of Figure 18 was obtained. The optimum value of pump power required

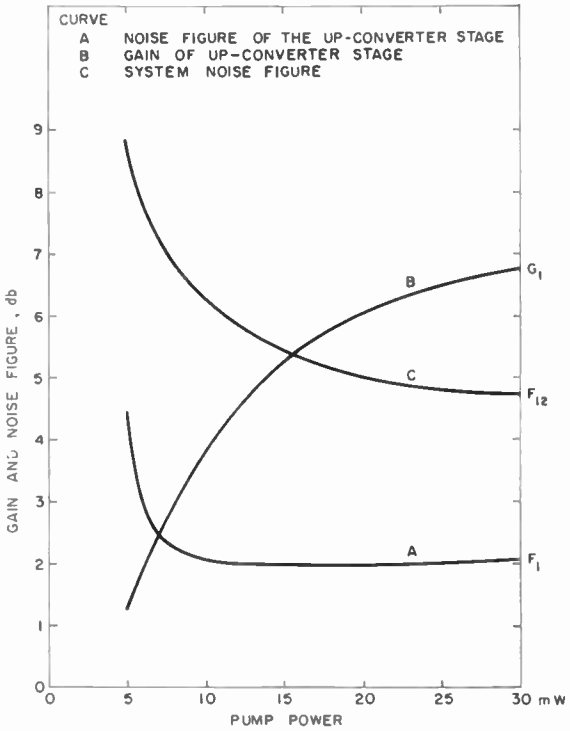


Fig. 19—Gain and noise figure of the up-converter with a MA4342A varactor diode. ($V_{BR} = 12$ volts)

for a minimum over-all system noise figure is approximately 10 milliwatts for the MA450F ($V_{BR} = 6$ volts) varactor diode. The increase in the noise figure of the up-converter stage with increasing pump power is believed to be due to reverse-current noise.

To show the effect of the reverse-current noise, another varactor diode with a higher reverse-breakdown voltage ($V_{BR} = 12$ volts) was used in the up-converter. Curve A of Figure 19 shows the measured first-stage noise figure as a function of the applied pump power using the MA4342A diode. In this case, the first-stage noise figure remains rather constant over the range of pump power applied to the diode.

The over-all system noise figure, shown by curve C of Figure 19, is slightly higher than that obtained in the previous case due to the reduced gain realized with this diode.

The measured values of gain and noise figure of the parametric up-converter compare reasonably well with the theoretical values previously calculated. Since the computed results are so dependent upon the value of γ chosen for the diode, the comparison of the computed and measured values of the performance characteristics is rather limited. A better comparison could be made if a more exact value of γ were obtained by means of a Fourier analysis of the capacitance–voltage characteristic and if a more precise value of the voltage drive on the varactor diode was determined by careful measurement.

Input Circuit Losses

With a sum-mode up-converter, no negative resistance is associated with the input circuit so that any loss connected with this circuit adds directly to the system noise figure and degrades the effective gain of the up-converter. To determine the total insertion loss due to the input circuit, the input voltage-standing-wave ratio was determined. The minimum standing-wave ratio occurs very close to the point where the over-all system noise figure is at a minimum. Similar results are obtained at other frequencies in the UHF range. The particular input circuit used was made to match a 50-ohm source. The loss associated with input voltage-standing-wave ratios of the magnitude shown in Curve D Figure 18 near the operating point is negligible. More significant are the ohmic losses in the input circuit which result in insertion losses in the order of 0.5 to 1.0 db over the 470 to 890 mc frequency range.

Bandwidth of Up-converter

In the up-converter structure used, the varactor diode loads the cavity quite heavily, so that the 3-db bandwidth of the idler circuit is about 1000 mc. Some of this loading is also due to the load provided by the down-converter. Due to the wide-band nature of the idler circuit response, the over-all tuner bandwidth, excluding the i-f characteristic, is determined largely by the bandwidth of the input circuit—approximately 10 mc. The idler-circuit bandwidth could be reduced by further decoupling of the varactor diode from the resonant cavity (through the use of a thicker iris between the pump and idler resonators). The wide-band characteristic of the idler circuit does not impair the noise figure and gain performance of the up-converter, although the image response is deteriorated.

Dynamic Range of Parametric Tuner

The dynamic range of the up-converter, including the saturation effects of the down-converter, is shown in Figure 20. This curve is a linear function of the input signal for input signals less than 30 dbm. Across a 300-ohm transmission line this would correspond to a signal of 17,300 microvolts. Additional dynamic range could be obtained by application of reverse bias to the varactor diode. With the up-converter

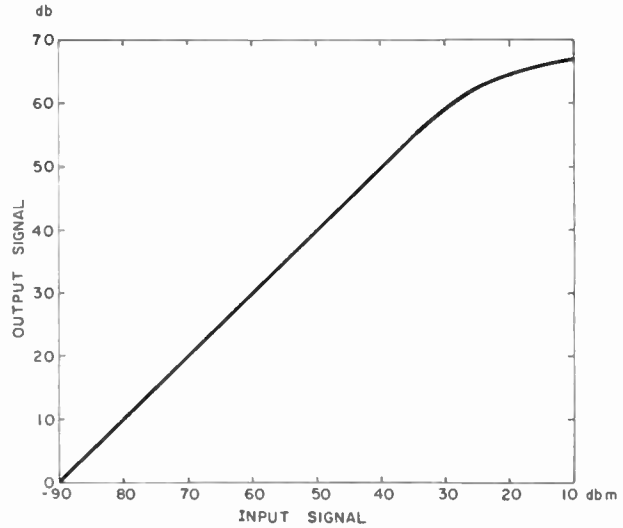


Fig. 20—The dynamic range of the up-converter and down-converter combination.

structure described, application of reverse bias can reduce the system gain by 20 db without appreciable detuning of the microwave circuits.

Other Characteristics

Further work on the parametric tuner would be necessary before the more detailed measurements are possible (e.g., spurious responses, frequency stability, tracking of microwave and VHF-UHF circuits, and cross modulation). Some previous work has been done in this area on the difference-mode up-converter; however, direct application of those results to the present tuner is probably not possible. Determina tion of such items as oscillator frequency stability must be delayed until a solid-state microwave source with sufficient power output is available.

Conclusions

A parametric tuner was developed and its feasibility for television receivers was investigated. The developed tuner was operated in a sum-mode and exhibited a noise figure of 4 db at 575 mc. Further reduction of the noise figure can be expected with improved varactor diodes. The tuner was designed to operate in the VHF and UHF bands. Consideration was given to cost and simplicity in manufacturing.

The feasibility of a parametric tuner depends on the availability of a low-cost microwave pump. This pump should preferably be a solid-state device such as a tunnel diode. At present, tunnel diodes are capable of operating at very high frequencies, but the power output in X-band is less than 1 milliwatt. Furthermore, means to tune and stabilize high-frequency (X-band) oscillators must be developed.

Appendix

Gain and Noise Measurements of the Upconverter Stage

The power gain of an amplifying stage is defined as the ratio of the output power P_2 to input power P_1. The maximum available power gain is realized when a matched condition exists at the input and output terminals. Since the input and output frequencies of a parametric upconverter differ widely, a convenient method of measuring the power gain is by means of a bolometer. The noise figure of the first stage can be computed using the stage gain and the measured values for the system noise figure and the down-converter noise figure. An alternative method of measuring the gain and stage noise figure was used in order to double check the results of measurements with the above described method. There was good correlation between the two methods. A new method was found to measure the first-stage noise figure and is described below.

The normal noise-measuring setup is shown in Figure 21. Under operating conditions, with switch S closed, the output meter will indicate a particular noise power output denoted N_{12}. Insertion of 3 db attenuation by opening the switch reduces the total noise power at the output to $N_{12}/2$. The noise figure of the system is then given by the amount of noise power required from the calibrated noise generator to restore the noise at the output to its original value of N_{12}. The system noise figure is expressed by

$$F_{12} = F_1 + \frac{F_2 - 1}{G_1}, \tag{13}$$

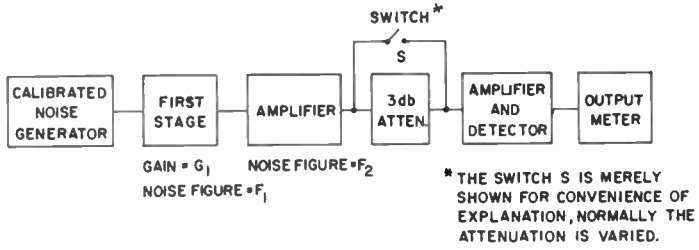


Fig. 21—Setup for noise measurement.

where F_{12} = system noise figure,

F_1 = first-stage noise figure,

F_2 = noise figure of second stage including any added noise from succeeding stages,

G_1 = first-stage available power gain.

The noise figure and the available power gain of a stage can be obtained from a set of noise-figure measurements conducted under specific conditions. Figure 22 shows the necessary equipment in block diagram form. In addition to the 3-db attenuator following the second stage, another attenuator has been inserted between the first and second stages. The first and second attenuators are labeled I and II in Figure 22. In these measurements, a particular value of attenuation is chosen for attenuator I and the corresponding noise figure is found by the normal method of measurement using attenuator II and the noise source.

If an attenuation ratio of M is inserted in attenuator I, the new system noise figure F_{12}' will be

$$F_{12}' = F_1 + \frac{MF_2 - 1}{G_1}. \tag{14}$$

The available power gain from Equations (13) and (14) is

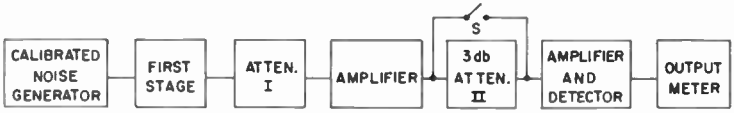


Fig. 22—Setup for noise measurement from which available gain can be obtained.

$$G_1 = \frac{F_2(M-1)}{F_{12}' - F_{12}}, \tag{15}$$

and the corresponding first-stage noise figure is given by

$$F_1 = F_{12} - \frac{(F_2 - 1)(F_{12}' - F_{12})}{F_2(M-1)}. \tag{16}$$

When $M = 2$, corresponding to 3-db attenuation, Equations (15) and (16) reduce to

$$G_1 = \frac{F_2}{F_{12}' - F_{12}}, \tag{15a}$$

and

$$F_1 = F_{12} - \frac{1}{F_2}(F_2 - 1)(F_{12}' - F_{12}). \tag{16a}$$

If Equation (14) is rewritten as

$$F_{12}' = F_1 - \frac{1}{G_1} + \frac{F_2}{G_1} M, \tag{17}$$

and the system noise figure F_{12}' plotted as a function of M, the slope of the resulting straight line will give the value of F_2/G_1. The gain G_1 can be obtained using the value of F_2. From the $M = 0$ intercept, $F_1 - (1/G_1)$, the first-stage noise figure can be obtained.

Alternative Method of Determining Noise Figure of First Stage

An alternative method of finding F_1 is as follows. The noise figure F is defined as

$$F = \frac{N_0}{GkT_0B}, \tag{18}$$

where N_0 = total available noise at the output,

G = available power gain of system,

k = Boltzmann's constant,

T_0 = absolute temperature in degrees Kelvin,

B = bandwidth in cycles per second.

The factor GkT_0B is equal to the available power at the output due to

the source resistance alone. At the output, the total available noise is then

$$N_0 = FGkT_0B. \tag{19}$$

Figure 23 shows a block diagram of the measuring scheme used. With the switch S closed, the noise at the output of the system shown in Figure 23 is given by

$$N_{12} = F_{12}GkT_0B. \tag{20}$$

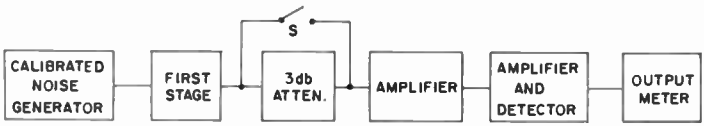


Fig. 23—Alternative setup for determining noise figure of first stage.

When the switch S in Figure 23 is opened, the output noise will be

$$N_{12}' = F_{12}'G'kT_0B, \tag{21}$$

where $G' = G/2$.

For a low-noise first stage, the noise power output with the switch S open will be less than that obtained with the switch closed. Let sufficient noise be added from the calibrated noise generator so that the output noise is restored to its original value, so that

$$N_{12} = N_{12}' + N_x \tag{22}$$

where N_x = noise at the output due to added noise at the input. This increment of noise power N_x, at the output can be expressed in terms of the corresponding noise figure F_x by

$$N_x = F_xG'kT_0B. \tag{23}$$

From Equations (20), (21), (22), and (23), we obtain the relation

$$GF_{12} = G'(F_{12}' + F_x), \tag{24}$$

or, since $G' = G/2$,

$$F_{12} = \frac{1}{2}(F_{12}' + F_x). \tag{25}$$

Using Equation (13)

$$F_{12} = F_1 + \frac{F_2 - 1}{G_1},$$

and Equation (14) ($M = 2$)

$$F_{12}' = F_1 + \frac{2F_2 - 1}{G_1},$$

in Equation (25), results in the expression

$$F_1 = F_x + \frac{1}{G_1}. \tag{26}$$

Thus, the first-stage noise figure is expressed in terms of the incremental noise figure F_x and the first-stage gain. For large first-stage gains, where $F_x \gg 1/G_1$,

$$F_1 \doteq F_x.$$

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First Quarter, 1963

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† Report all corrections to *RCA Review*, RCA Laboratories, Princeton, N. J.

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"Comparative Study of Low VHF, High VHF, and UHF Television Broadcasting in New York Area," D. W. Peterson, *Broadcast News* (February) 1963
"Efficient High-Level Parametric Frequency Converters," B. S. Perlman and B. B. Bossard, *Proc. IEEE* (Correspondence) (February) 1963
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"Measured Values of Noise Spectra, *S* and II, of Ultra-Low-Noise Beams," J. M. Hammer, *Proc. IEEE* (Correspondence) (February) 1963
"Megawatt UHF Test Station," *Broadcast News* (February) 1963
"Metal-Semiconductor Barrier Height Measurement by the Differential Capacitance Method—One Carrier System," A. M. Goodman, *Jour. Appl. Phys.* (February) 1963
"Noise on a Drifting Maxwellian Beam," S. Bloom and B. Vural, *Jour. Appl. Phys.* (February) 1963
"RCA 50 KW UHF Transmitter," *Broadcast News* (February).... 1963
"RCA 12.5 and 25-Kilowatt UHF Transmitters," *Broadcast News* (February) 1963
"Recent Developments in Color-Television Camera Equipment," H. N. Kozanowski and S. L. Bendell, *Trans. IEEE PGB* (February) 1963
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"Improving Pulse Rise Time With Snap-Off Diodes," K. C. Hu, *Electronics* (February 15) 1963
"Optical Absorption Spectrum of Metal-Free Phthalocyanine Single Crystals," G. H. Heilmeier and G. Warfield, *Jour. Chem. Phys.* (February 15) 1963
"Photoconductivity in Metal-Free Phthalocyanine Single Crystals," G. H. Heilmeier and G. Warfield, *Jour. Chem. Phys.* (February 15) 1963
"Arc-Protection Circuits," D. D. Mawhinney, *Electronics* (February 22) 1963
"Camera Tubes for Studio Use—A Semi-Technical Appraisal for Educators," J. W. Wentworth, *Jour. S.M.P.T.E.* (March)... 1963
"Comparative Study of Low-VHF, High-VHF, and UHF Television Broadcasting in the New York City Area," D. W. Peterson, *RCA Review* (March) 1963
"An Electron-Beam Machine," A. B. El-Kareh, *RCA Review* (March) 1963
"High-Speed Arithmetic Employing Tunnel Diodes," H. S. Miiller, *RCA Review* (March) 1963
"#66 Parallel-Resistance Nomograph," L. J. Striednig, *Electronic Industries* (Engineer's Notebook) (March) 1963

"The Optical Tunnel—A Versatile Electro-optical Tool," L. J. Krolak and D. J. Parker, *Jour. S.M.P.T.E.* (March) 1963
"Scale Model Investigations of Electromagnetic Wave Propagation Over Natural Obstacles," M. P. Bachynski, *RCA Review* (March) 1963
"A Statistical Approach to Electromagnetic Interference of Rotating Radars," A. Arcese, *Trans. IEEE PGRFI* (March) 1963
"Unconditional Stability in Tunnel-Diode Amplifiers," A. S. Clorfeine, *RCA Review* (March) 1963
"Fitting a Wide-Band Signal Into a Narrow-Band Receiver," S. Kallus, B. Rabinovici, and A. Newton, *Electronics* (March 8).... 1963

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